Boy in Well

Design By Erik Vincent

A simple DIY project featuring the ever popular delay chip, the PT2399. Boasting up to 600ms of delay time with a respectable “vintage” tone, the Boy In Well Delay features 3 dial controls, Time, Level and Repeats and is a well suited delay project for the beginner.

The boy in well is an affordable DIY delay and is suited to a 1590B and can be built with common “off the shelf” parts.
# Bill of Materials, Stock Boy in Well

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>Resistor</th>
<th>ICs</th>
<th>Diode</th>
<th>Potentiometer</th>
</tr>
</thead>
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<tr>
<td>C1 100μF (Electrolytic)</td>
<td>R1 10K</td>
<td>U1 78L05</td>
<td>U2 PT2399</td>
<td>Time 50kb (16mm)</td>
</tr>
<tr>
<td>C2 47μF (Electrolytic)</td>
<td>R2 10K</td>
<td></td>
<td>U3 TL072</td>
<td>Level 50kb (16mm)</td>
</tr>
<tr>
<td>C3 100nF (film)</td>
<td>R3 2.7K</td>
<td></td>
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<tr>
<td>C4 47μF (Electrolytic)</td>
<td>R4 10K</td>
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<td></td>
<td></td>
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<tr>
<td>C5 47μF (Electrolytic)</td>
<td>R5 10K</td>
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<tr>
<td>C6 100nF (film)</td>
<td>R6 20K</td>
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<tr>
<td>C7 100nF (film)</td>
<td>R7 1K</td>
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<td>C8 100nF (film)</td>
<td>R8 10K</td>
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<td>C9 100nF (film)</td>
<td>R9 10K</td>
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<tr>
<td>C10 15nF (film)</td>
<td>R10 1M</td>
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<td>C11 2.2nF (film)</td>
<td>R11 180K</td>
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<td>C12 10nF (film)</td>
<td>R12 360K</td>
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<tr>
<td>C13 2.2nF (film)</td>
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<td>C14 4.7nF (film)</td>
<td>R14 10K</td>
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<td>C15 220nF (film)</td>
<td>R15 20K</td>
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<td>C16 47pF (ceramic)</td>
<td>R16 12K</td>
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<td>C17 1μF (Electrolytic)</td>
<td>R17 1K</td>
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<td>C18 1μF (Electrolytic)</td>
<td>R18 100K</td>
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<tr>
<td>C19 100pF (ceramic)</td>
<td>R19 2K</td>
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<tr>
<td>C20 1μF (Electrolytic)</td>
<td>R20 5.1K</td>
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<tr>
<td>C21 1μF (Electrolytic)</td>
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<tr>
<td>C22 47nF (film)</td>
<td></td>
<td>U1 78L05</td>
<td>U2 PT2399</td>
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<tr>
<td>C23 22nF (film)</td>
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<td></td>
<td>U3 TL072</td>
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<td>D1 1N4001</td>
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</table>
PCB Spacing
The Boy in Well PCB is spaced for 1590B sized enclosures or larger
Pot Spacing
The Boy in Well PCB mounted potentiometers are spaced for Alpha 16mm potentiometers

Modifications
Following is a couple of worthwhile modifications that can be applied to the Boy in Well.

Resistors
Changing the values of R12 and R11, keeping R12 as the larger value, will increase or decrease the gain created at the input of the signal. At a 2:1 ratio, this creates a voltage gain of 2, or 6dB. Creating a ratio of resistance between R12 and R11 of 3:1 will create a voltage gain of 3, or 9.5dB, 4:1 of 4 or 12dB, and so on. If too much noise is causing mild distortion to the dry signal, creating a ratio of 1:1 creates unity, or 0dB.

The sum of resistance between R3 and the Time pot sets the amount of delay between notes. The lesser the resistance, the shorter in times of delay, getting into reverb/slapp-back territory. The greater the resistance, the longer pauses between delays. Remember that a minimum of 2K of resistance is required on the first 400ms of power-up time for the PT2399, so try to keep it above that mark unless a timing method is added off-board. See the chart in section 4.2 for resistance values and delay times.

Capacitors
C8 and C9 control the harmonics of the delay signal. Lowering the values of C8 and C9 will allow more high harmonics to go through the chip. If you are using the PT2399 to do short delay/echo you can go as low as 22nF for C8 and C9, for longer delays (300ms) do not go lower than 47nF (100nF seems to be a good value for long delays).

C13 and C14 control the MFB low pass filter for processing the delays. Increasing their capacitance will lower the frequency cut off rate, while lowering it will increase the frequency cut-off rate. Values between 330pF – 5600pF can be used.

Voltage Regulators
Adapting the Jack Orman’s NYE mod, changing the Linear Regulator from a 5V LDO to a 6V LDO such as a 78L06, can make the PT2399 give off a cleaner sounding delay by overclocking the PT2399’s internal oscillator. This is just a warning about overclocking. The max voltage for the PT2399 is listed as 5.5V but really pops a little over 6V, so this is pushing the chip to its maximum. Thankfully, due to voltage drops after the regulator, it keeps the circuit relatively safe. Do at your own risk.
Boy in Well Circuit Analysis for modifying purposes.

1. Boy in Well Circuit.
The Boy in Well schematic can be broken down into some simpler blocks: Power Supply, Input Buffer and Gain Stage, PT2399 Stage, and Output Buffer.

The circuit is designed around a Princeton Technology Corp PT2399 CMOS echo/delay processor with built in ADC, 44Kb of internal RAM, and a DAC.

The input impedance on the Boy in Well is close to 1M Ω, allowing the pedal to not overload the pickups on the guitar or to tone suck.

The Power Supply Stage provides the electrical power and bias voltage to all the circuitry, the whole power consumption is low and estimated around 8mA:

- The diode D1 protects the pedal against adapter reverse polarity connections.

- The resistor voltage divider composed by R1 and R2 generates 4.5V to be used as a bias voltage/virtual ground. The resistors junction (+4.5V) is decoupled to ground with a large value electrolytic capacitor C4 47μF.

- The capacitor C1 is a large electrolytic capacitor to remove ripple from the power supply.

- The LP2950-50LPRE3 is an efficient LM7805 style 5V linear regulator. It is a good idea to get the input capacitor (C1) and output capacitors (C2 & C3) as close to it as possible. It is also a good design rule to get C3 as close to the PT2399, keeping the 5V path short to reject DC line noise. Pairing the C2 electrolytic with the C3 film capacitor helps as electrolytic capacitors are slower in response than film and ceramic capacitors.
3. Input Buffer and Gain Stage.
The first stage is made of an inverting op-amp amplifier with a fixed voltage gain and some filters to shape the gain response and high input impedance that preserves signal quality eliminating tone sucking (high-frequency loss):

The 1MΩ R10 resistor from the input to ground is an anti-pop resistor, it will avoid abrupt pop sounds when the effect is engaged.

The 220nF C15 input capacitor blocks DC and provides simple high pass filtering. C15 and R11 create a high pass filter.

\[
C_{15} = \frac{1}{2\pi R11 C15} \\
C_{15} = \frac{1}{2\pi \cdot 180K \cdot 220nF} \\
C_{15} = \frac{1}{2\pi \cdot 180,000 \cdot 0.00000022} \\
C_{15} = 4.02 \text{ Hz}
\]

With a cut of 4Hz it will block DC and any low-frequency parasitic oscillation.

3.1 Input Impedance.
The input impedance is defined by the formula:

\[
Z_{in} = R10 \parallel (R11 + Z_{in TL072})
\]

If you look up the datasheet for the TL072, under the electrical characteristics, the input resistance is \(10^{12}\)

\[
Z_{in} = 1,000,000 \parallel (180,000 + 1,000,000,000,000) \\
Z_{in} = 1,000,000 \parallel 1,000,000,180,000 \\
Z_{in} = 999,999\,\Omega
\]

Therefore, the Boy in Well input resistance is a hair under 1M, which is pretty ideal. This will definitely make sure tonesucking will not occur with any long cables and that the guitar pickups will not become overloaded.
3.2 Voltage Gain.
The voltage gain is set between the values of R11 and R12, so in a non-inverting topology this can be calculated as:

\[ G_v = \frac{R_{12}}{R_{11}} \]

\[ G_v = \frac{360,000}{180,000} = 2 \text{ (6dB)} \]

3.3 Low Pass Filtering.
The small 47pF capacitor C16 across the feedback resistor works as a low pass filter, softening the corners of the guitar waveform and mellowing out the high end before the clipping.

The cut-off frequency of the filter is defined by the formula:

\[ f_c = \frac{1}{(2\pi \cdot R_{12} \cdot C_{16})} \]

\[ f_c = \frac{1}{(2\pi \cdot 360,000 \cdot 0.000000000047)} = 9.411 \text{ kHz} \]

This filter cuts off any high frequency harmonics that might occur from a distorted signal that might have been created from the 6dB gain. Not a guarantee that there will be distortion, but if there was, this will filter much of it.
4. The PT2399 Stage.
This stage is taking the prepared buffered audio signal and does all the delaying before outputting the delayed and repeated signal:
4.1 The PT2399 Power Supply

The first 4 pins of the PT2399 are the power supply for the IC:

- **Pin 1** takes in power generated from 5V linear-regulator, U1. The PT2399 can officially handle supply voltages between 4.5V and 5.5V. Some folks have reported success at 6V, but because this would be overclocking and going over the recommended max, it would be important to note if 6V is possible, you don’t want to go much higher than that.

- **Pin 2** is the Ref pin formed by an internal voltage divider of 2x 6K resistors. This creates a voltage reference that is half of the input voltage and is used to create a virtual ground inside the PT2399 and function as a bias reference voltage for its internal VCO circuit. Like a typical pedal circuit, this voltage reference is decoupled to ground with a large value electrolytic capacitor C5 47uF.

- **Pin 3** is the analog ground for the PT2399. This creates ground for the internal VCO, internal Op Amps, and internal comparator inside the PT2399. By using a ground plane on the PCB, we keep a very short, but thick trace between Pin 3 and Pin 4.

- **Pin 4** is the digital ground for the PT2399. It is internally connected to analog ground via an approximate 10 ohms of resistance. This creates ground for the delay propagating circuitry. By using a ground plane on the PCB, we keep a very short, but thick trace between Pin 3 and Pin 4.
4.2 The PT2399 Voltage Controlled Oscillator

Pins 5 and 6 make up the output and input of the VCO or Voltage Controlled Oscillator:

- **Pin 5** is the system clock output pin. The output of this pin is a square wave with a frequency based off the delay time. At its shortest delay, the square wave is at 22 MHz, which is a delay of approximately 30ms. At its longest delay, the square wave is at 2 MHz, which is a delay of approximately 340ms. The signal is approximately 5 Vpp, but it will increase as the frequency decreases and decrease as the frequency increases. This can be used as a feedback for measuring precise delay as simply changing the resistance on Pin 6 will not give an exact delay value. As this is high frequency (22 MHz potentially), a pre-scaler may be desired to read this output from the PT2399 VCO. This would most likely be something good for a microcontroller that could visually display the delay times. This would also be useful to read if trying to synchronize the delay with some other equipment. It is also possible to override the VCO with an external source.

- **Pin 6** is the VCO frequency adjustment pin. The voltage at this pin is always 2.5V and using an external resistor to ground the current will change that will result in a VCO variation and delay time change.

Find below a table with the relationship between Pin 6 resistance to ground, internal clock frequency, delay time and THD. The table is indicative, as the values vary from chip to chip, however it is a good starting point.

<table>
<thead>
<tr>
<th>R</th>
<th>27.6 k</th>
<th>21.3 k</th>
<th>17.2 k</th>
<th>14.3 k</th>
<th>12.1 k</th>
<th>10.5 k</th>
<th>9.2 k</th>
<th>8.2 k</th>
<th>7.2 k</th>
<th>6.4 k</th>
</tr>
</thead>
<tbody>
<tr>
<td>f clock</td>
<td>2.0 M</td>
<td>2.5 M</td>
<td>3.0 M</td>
<td>3.5 M</td>
<td>4.0 M</td>
<td>4.5 M</td>
<td>5.0 M</td>
<td>5.5 M</td>
<td>6.0 M</td>
<td>6.5 M</td>
</tr>
<tr>
<td>Delay</td>
<td>342 ms</td>
<td>273 ms</td>
<td>228 ms</td>
<td>196 ms</td>
<td>171 ms</td>
<td>151 ms</td>
<td>137 ms</td>
<td>124 ms</td>
<td>114 ms</td>
<td>104 ms</td>
</tr>
<tr>
<td>THD</td>
<td>1%</td>
<td>0.80%</td>
<td>0.63%</td>
<td>0.53%</td>
<td>0.46%</td>
<td>0.41%</td>
<td>0.36%</td>
<td>0.33%</td>
<td>0.29%</td>
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<tr>
<td>R</td>
<td>5.8 k</td>
<td>5.4 k</td>
<td>4.9 k</td>
<td>4.5 k</td>
<td>4.0 k</td>
<td>3.4 k</td>
<td>2.8 k</td>
<td>2.4 k</td>
<td>2.0 k</td>
<td>1.67 k</td>
</tr>
<tr>
<td>f clock</td>
<td>7.0 M</td>
<td>7.5 M</td>
<td>8.0 M</td>
<td>8.5 M</td>
<td>9.0 M</td>
<td>10 M</td>
<td>11 M</td>
<td>12 M</td>
<td>13 M</td>
<td>14 M</td>
</tr>
<tr>
<td>Delay</td>
<td>97 ms</td>
<td>92 ms</td>
<td>86 ms</td>
<td>81 ms</td>
<td>76 ms</td>
<td>68 ms</td>
<td>62 ms</td>
<td>57 ms</td>
<td>52 ms</td>
<td>48 ms</td>
</tr>
<tr>
<td>THD</td>
<td>0.25%</td>
<td>0.25%</td>
<td>0.23%</td>
<td>0.22%</td>
<td>0.21%</td>
<td>0.19%</td>
<td>0.18%</td>
<td>0.16%</td>
<td>0.15%</td>
<td>0.15%</td>
</tr>
<tr>
<td>R</td>
<td>1.47 k</td>
<td>1.28 k</td>
<td>1.08 k</td>
<td>0.894</td>
<td>0.723</td>
<td>0.519</td>
<td>0.288</td>
<td>0.5</td>
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</tr>
<tr>
<td>f clock</td>
<td>15 M</td>
<td>16 M</td>
<td>17 M</td>
<td>18 M</td>
<td>19 M</td>
<td>20 M</td>
<td>21 M</td>
<td>22 M</td>
<td>22 M</td>
<td>22 M</td>
</tr>
<tr>
<td>Delay (ms)</td>
<td>46 ms</td>
<td>43 ms</td>
<td>41 ms</td>
<td>38 ms</td>
<td>37 ms</td>
<td>34 ms</td>
<td>33 ms</td>
<td>31 ms</td>
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</tr>
<tr>
<td>THD</td>
<td>0.15%</td>
<td>0.14%</td>
<td>0.14%</td>
<td>0.14%</td>
<td>0.13%</td>
<td>0.13%</td>
<td>0.13%</td>
<td>0.13%</td>
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</tr>
</tbody>
</table>

**Note:** The THD (Total Harmonic Distortion) is higher with longer delay times, as the signal goes degraded with a lower sampling rate. Using delays over 350ms can cause audible distortion.

**Note:** The voltage on pin 6 is constant (2.5V) but the current flowing out of it current has a linear relationship with the delay time. The practical delay range of the chip is from about 35 msecs to 600 msecs, so this gives a current of between 5.4mA and 50uA.

Pin 6 current (mA) = \( \frac{28.65}{\text{Delay msecs} - 29.70} \)

**Note:** If delay resistance from Pin 6 to ground is less than 2KΩ during the power-on of the PT2399, the chip may latch up, causing the chip to crash and stop functioning. If a very short delay time is required, ensure that the delay resistance is greater than 2KΩ for the first 400ms after power on. After the first 400ms, the Pin 6 resistance to ground can go as low as needed.

**Controlling the Delay Time:** Between VR1, a 50K potentiometer and R3, a 2.7K resistor, a minimum resistance of 2.7K is achieved preventing a lock-up of the PT2399 at power on and a maximum delay of 52.7K creating a range of delay between 60ms and 633ms. These can be calculated by:

\[
\begin{align*}
\text{Delay}_\text{msecs MIN} &= (0.01146 \cdot (VR1 + R3)) + 29.70 \\
\text{Delay}_\text{msecs MIN} &= (0.01146 \cdot 2,700) + 29.70 \\
\text{Delay}_\text{msecs MIN} &= 30.942 + 29.70 = 60.642 \text{ ms}
\end{align*}
\]

\[
\begin{align*}
\text{Delay}_\text{msecs MAX} &= (0.01146 \cdot (VR1 + R3)) + 29.70 \\
\text{Delay}_\text{msecs MAX} &= (0.01146 \cdot 52,700) + 29.70 \\
\text{Delay}_\text{msecs MAX} &= 603.942 + 29.70 = 633.642 \text{ ms}
\end{align*}
\]

If using an external microcontroller with a digital potentiometer, such as the TAP-FLO and Tap Tempo, so long as the microcontroller takes into consideration power on time and latch potential due to low resistances, after a successful power on, making R3 as small as 100 ohms is possible giving a minimum delay of close to 30 ms.
4.3 PT2399 Input Stage.
The PT2399 Input Stage consists of 3 op-amps. Two of them (2 and 3) are always used as part of the Sigma-Delta ADC circuit, so the designer cannot use them freely. The first op-amp is available to be used under any configuration, but the most common option is to use it as a filter/adder in a Multi-Feedback topology:
The first op-amp will filter the input stage removing the excess of high harmonics using a Multi-Feedback topology (MFB aka Infinite-Gain Multiple-Feedback):

The Multi-Feedback op-amp uses 2 poles (MFB-2) that give -12dB/octave of attenuation to the high-frequencies. The final filter (R5 and C3) adds an extra pole, making the total filter -18dB/octave. The MFB topology gives high gain / high Q with the inconvenient of more complex design calculations.

The MFB performs as good as a Sallen & Key filter (S&K uses 1 component less for unity gain filters though) but the MFB topology is chosen in this case it allows the op-amp to work as a summing amplifier, accepting a feedback path of the ECHO circuit.

There are several ways to calculate the values for the filter. Following the simple Elliot Sound Products method, it can be done like this:

R1=R14, R2=R9, R3=R8, C1=C14, and C2=13

R1=10K, R2=10K, R3=10K, C1=4.7nF, and C2=2.2nF

\[ f_c = \frac{1}{2\pi \sqrt{R_8 \cdot R_9 \cdot C_{13} \cdot C_{14}}} \]
\[ f_c = \frac{1}{2\pi \sqrt{10,000 \cdot 10,000 \cdot 0.0000000022 \cdot 0.0000000047}} \]
\[ f_c = \frac{1}{2\pi \sqrt{0.000000001034}} \]
\[ f_c = \frac{1}{0.0002020413} = 4949 \text{ Hz} \]
4.4 PT2399 Output Stage.
The output stage consists of 2 op-amps. The first one has limited functionality and it is used as a low pass filter after the Demodulator (Anti-Aliasing Filter). The second op-amp is freely available and is again usually configured in a Multi-Feedback op-amp filter.

The output stage uses 1 op-amp as the Demodulator low-pass filter. This Reconstruction Filter will smooth the analog signal created by the Demodulator.

The C9 (and C8) Capacitor forms a low pass filter in order to reduce the unwanted hi-frequencies, the PT2399 datasheet suggests 100nF for delay and 82nF for the echo. There is not much info about the functionality of these caps. Lowering the values of C8 and C9 will allow more high harmonics to go through the chip and therefore a "more natural sound", of course, the drawback would be more digital noise into the signal. If you are using the PT2399 to do short delay/echo you can go as low as 22nF for C8 and C9, for longer delays (300ms) do not go lower than 47nF (100nF seems to be a good value for long delays).

Using 100nF on C8/C9, makes the delayed signal harmonics above 1kHz to be attenuated (see Frequency Response section), it is not catastrophic as the natural sound of a delayed/echoed signal has intrinsically less high content (real echoes usually have a rapidly diminishing high frequency content, as these harmonics are absorbed easily by the walls and air). A good middle ground value to allow more harmonics and less high frequency noise into the circuit would be 68nF.

The second op-amp is again in the Multi Feed Back topology (MFB), it will clean and smooth the signal even more.

R7 and C12 form a last low pass filter with a cut frequency of 15.9kHz (using a 1KΩ resistor and a 10nF cap) The drawback of this last filter is that it will raise the output impedance of the circuit, this can be solved by using a more sensible RC combination, with a smaller R and a higher C (like 10Ω and 4.7u that give fc=3.3kHz). Thankfully, there is an output buffer that makes this issue mostly irrelevant.

C21 is the output cap that removes any DC level from the output, any big value (1 - 10uF or similar) will work.
5. Output Buffer.
The Output Buffer is the complement of the Input Buffer. It is also implemented over the TL072 dual op-amps and designed to attenuate the magnitude of the high frequencies with respect to the mid-low frequencies. This filter takes the unnatural sounding pre-emphasized audio and turns it back into its original response.

The op-amp is configured in the classic summing amplifier topology. The dry signal coming over R13 has a little more resistance than the dry signal coming in over R15, making the mix ratio 1.1:1 in favor of the wet signal.

5.1 Tone Frequency Response.
A low pass filter is created with R16 and C19.

\[
fc = \frac{1}{(2\pi \cdot R_{16} \cdot C_{19})}
\]

\[
f_c = 1 / (2\pi \cdot 12,000 \cdot 0.00000000001) = 132.7 \text{ kHz}
\]

The small 100p C19 capacitor across the feedback loop works as a low pass filter, mellowing out the high end of the signal and limiting the bandwidth which is a classic arrange in stomp boxes input stages that also maintain HF stability.

The Output capacitor C20 acts like a high pass filter together with R17 and R18. Being that R18 is larger than R17, the cut-off frequency is:

\[
fc = \frac{1}{(2\pi \cdot R_{18} \cdot C_{20})}
\]

\[
f_c = 1 / (2\pi \cdot 100,000 \cdot 0.000001) = 1.59 \text{ Hz}
\]

This acts to remove DC and any really low frequencies from the output signal.
5.2 Output Impedance.

The input impedance is defined by the formula:

The output resistor network composed by R17 and R18 will limit the output current; even if the output jack is connected to ground the op-amp will see a load of at least 1KΩ, limiting the output current and protecting the operational amplifier. The TL072 op-amp has an internal output resistance of around 100Ω.

The output impedance is defined by the formula:

\[ Z_{in} = R_{18} \parallel (R_{17} + Z_{in\text{TL072}}) \]

If you look up the datasheet for the TL072, under the electrical characteristics, the input resistance is \(10^{12}\)

\[ Z_{in} = 100,000 \parallel (1,000 + 100) \]
\[ Z_{in} = 100,000 \parallel 1,100 \]
\[ Z_{in} = 1,088Ω \]

1.088KΩ is good output impedance, keeping signal fidelity. It is a good practice to keep output resistance of a pedal below 10KΩ.
Testing Your Effect

Using alligator clips or soldering directly, wire your effect as in the following...

Input and Output Sockets

Pay close attention to the lugs of your sockets. Look at them side on so that you can distinguish the sockets individual layers. For instance the tip lug is connected to tip contact. The stereo jack looks the same as the socket below except it has an extra lug and contact for “Ring”.

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Off Board Wiring Diagram

Using a non-switched Miniature DC Jacks and 2 Mono Jacks

Mono Jack
Input Jack Shield
Input Jack Tip

Miniature DC Jack

Effect PCB
www.diyguitarpedals.com.au

Mono Jack
Output Jack Shield
* Left empty if using a metal enclosure

Mono Jack
Output Jack Tip

3pdt

In
Ground
+9v
Out

CLR
LED