Boy in Well

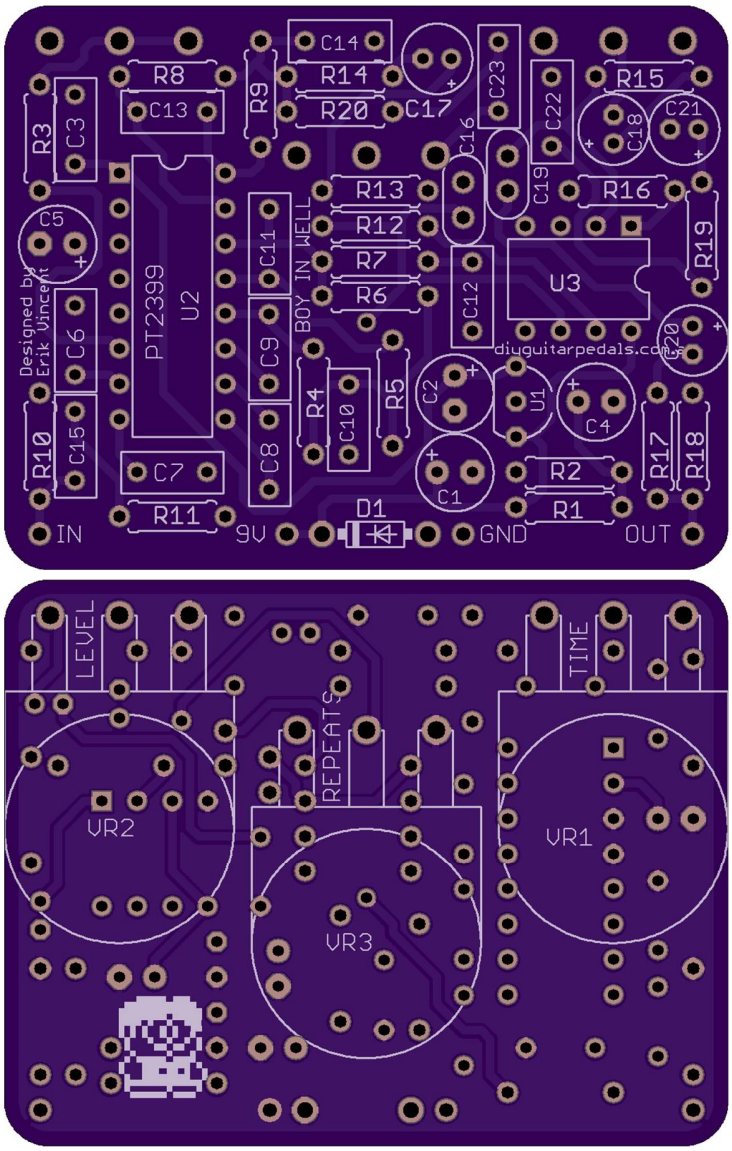
Design By Erik Vincent

A simple DIY project featuring the ever popular delay chip, the PT2399. Boasting up to 600ms of delay time with a respectable "vintage" tone, the Boy In Well Delay features 3 dial controls, Time, Level and Repeats and is a well suited delay project for the beginner.

The boy in well is an affordable DIY delay and is suited to a 1590B and can be built with common "off the shelf" parts.

Bill of Materials, Stock Boy in Well

Capacitor		Resistor	
C1	100µF (Electrolytic)	**R1**	10K
C2	47µF (Electrolytic)	**R2**	10K
C3	100nF (film)	**R3**	2.7K
C4	47µF (Electrolytic)	**R4**	10K
C5	47µF (Electrolytic)	**R5**	10K
C6	100nF (film)	**R6**	20K
C7	100nF (film)	**R7**	1K
C8	100nF (film)	**R8**	10K
C9	100nF (film)	**R9**	10K
C10	15nF (film)	**R10**	1M
C11	2.2nF (film)	**R11**	180K
C12	10nF (film)	**R12**	360K
C13	2.2nF (film)	**R13**	22K
C14	4.7nF (film)	**R14**	10K
C15	220nF (film)	**R15**	20K
C16	47pF (ceramic)	**R16**	12K
C17	1µF (Electrolytic)	**R17**	1K
C18	1µF (Electrolytic)	**R18**	100K
C19	100pF (ceramic)	**R19**	2K
C20	1µF (Electrolytic)	**R20**	5.1K
C21	1µF (Electrolytic)		
C22	47nF (film)	**ICs**	
C23	22nF (film)	**U1**	78L05
		U2	PT2399
Diode		**U3**	TL072
D1	1N4001		
		Potentiometer	
		Time	50kb (16mm)
		Level	50kb (16mm)
		Repeats	50kb (16mm)



PCB Spacing
The Boy in Well PCB is spaced for 1590B sized enclosures or larger

Pot Spacing
The Boy in Well PCB mounted potentiometers are spaced for Alpha 16mm potentiometers

Assembly.

1. Soldering Order.

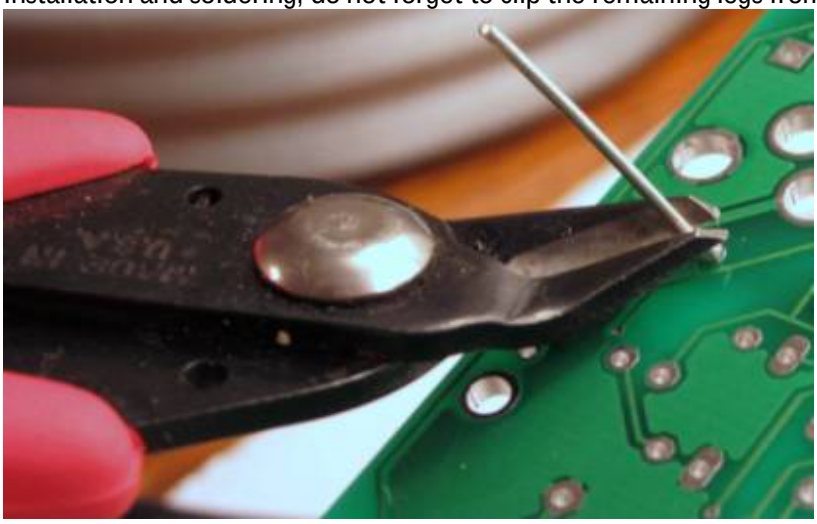
When soldering things to the PCB, the idea is to solder things on from lowest profile to tallest.

For the Boy in Well, the best order would be: resistors, diodes, ceramic capacitors, IC sockets (if socketing), voltage regulators, ICs (if not socketing), film capacitors, electrolytic capacitors, wiring, potentiometers.

1.1 Resistors.

Resistors are small passive components designed to create a resistance of passage of an electric current.

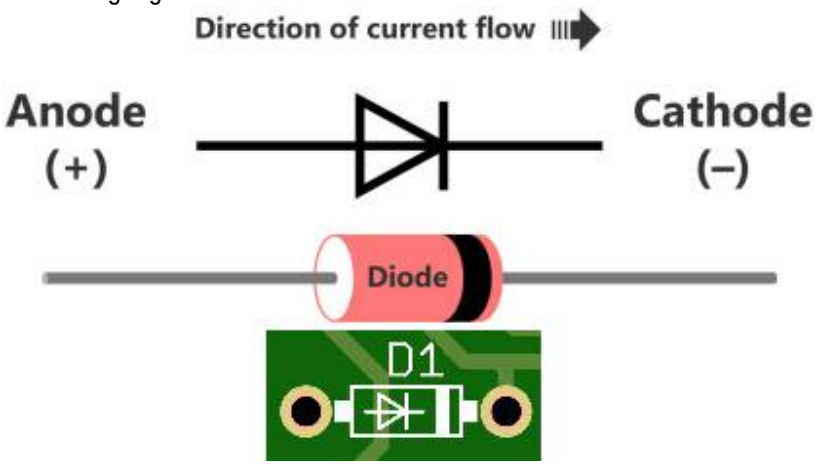
For this pedal we will be using 1/4 Watt resistors. These can either be 5% tolerance carbon resistors, or 1% tolerance metal film resistors. Orientation of “which way is up” doesn’t matter, so you can install them either way. After installation and soldering, do not forget to clip the remaining legs from the PCB.



1.2 Diodes.

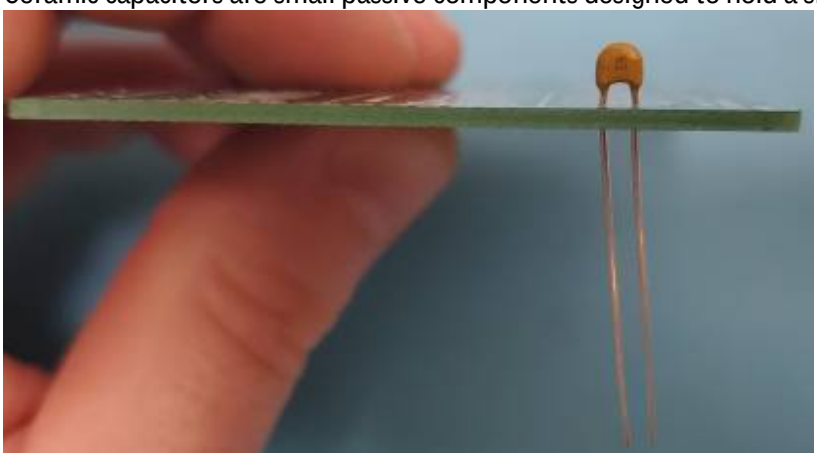
Diodes are semiconductor components typically designed to allow the flow electric current to go in one direction only.

The orientation of a diode does matter based on the cathode and anode of the diode in the circuit. Make sure the stripe on the diode lines up with the stripe on the PCB's silkscreen. After installation and soldering, do not forget to clip the remaining legs from the PCB.



1.3 Capacitors (ceramic).

Ceramic capacitors are small passive components designed to hold a small amount of charge in a circuit.



Orientation of "which way is up" doesn't matter, so you can install them either way. After installation and soldering, do not forget to clip the remaining legs from the PCB.

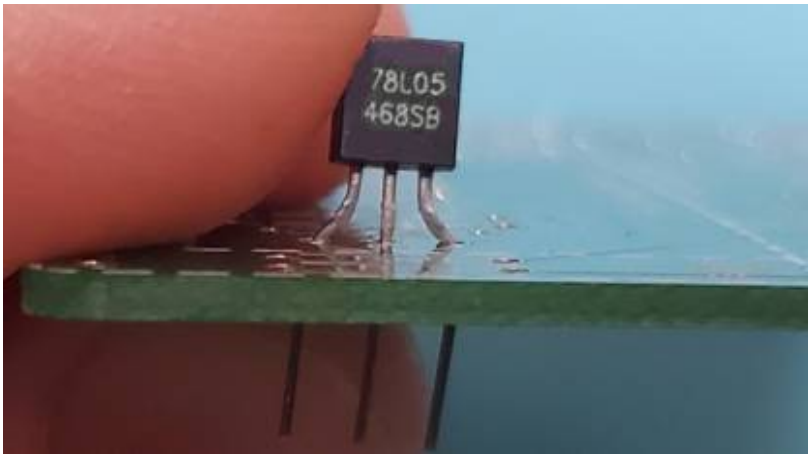
1.4 IC Sockets.

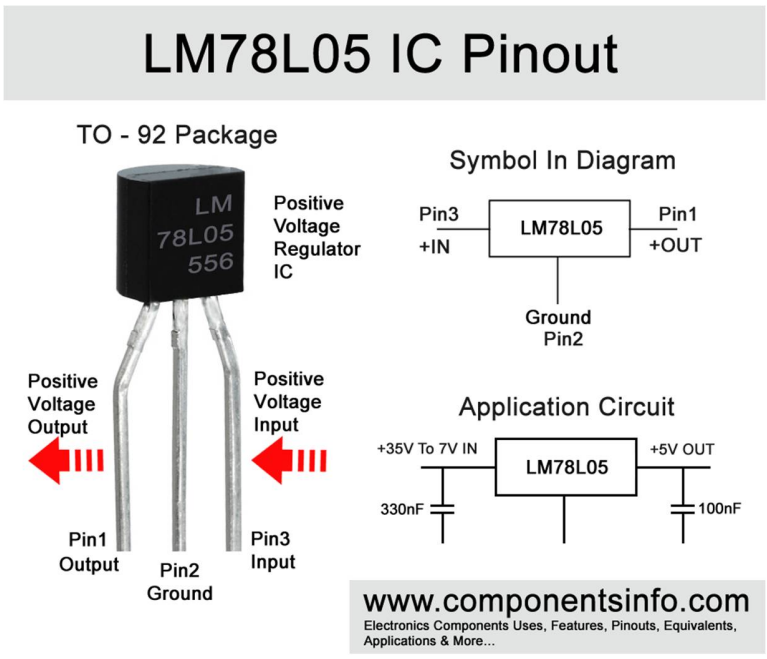
These are holders that allow easy installation and uninstallation of ICs.

These devices will have a silk screen notch to indicate an orientation with the IC or socket for the IC. Just make sure the IC notches match.

1.5 Voltage Regulator.

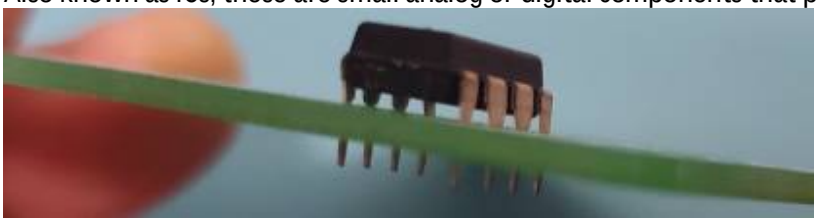
These are three-legged linear voltage regulators in a packaged called a TO-92 package. They take a larger voltage and drop it to a smaller one.





1.6 Integrated Circuits.

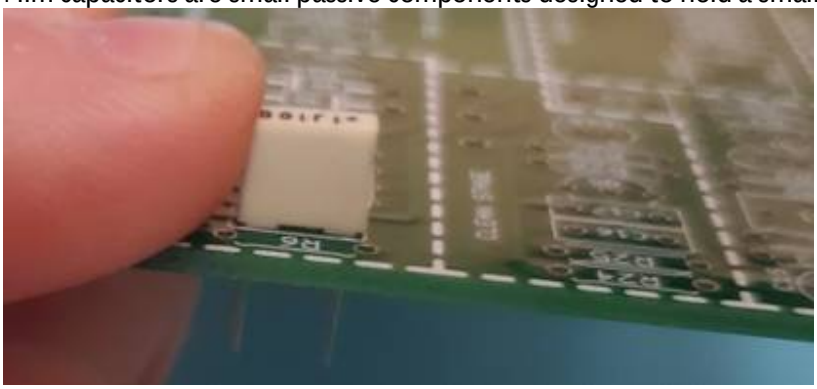
Also known as ICs, these are small analog or digital components that provide specific electrical functions.



Orientation of “which way is up” will be indicated by a notch on the silkscreen on the PCB and a dot or bar on the actual IC itself. Do make sure they match.

1.7 Capacitors (film).

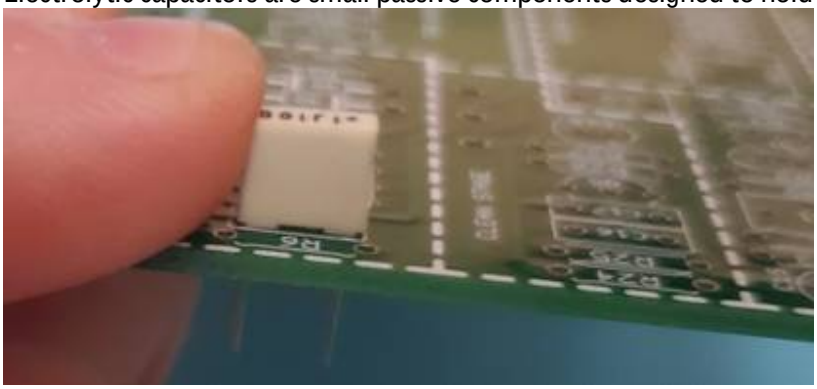
Film capacitors are small passive components designed to hold a small amount of charge in a circuit.



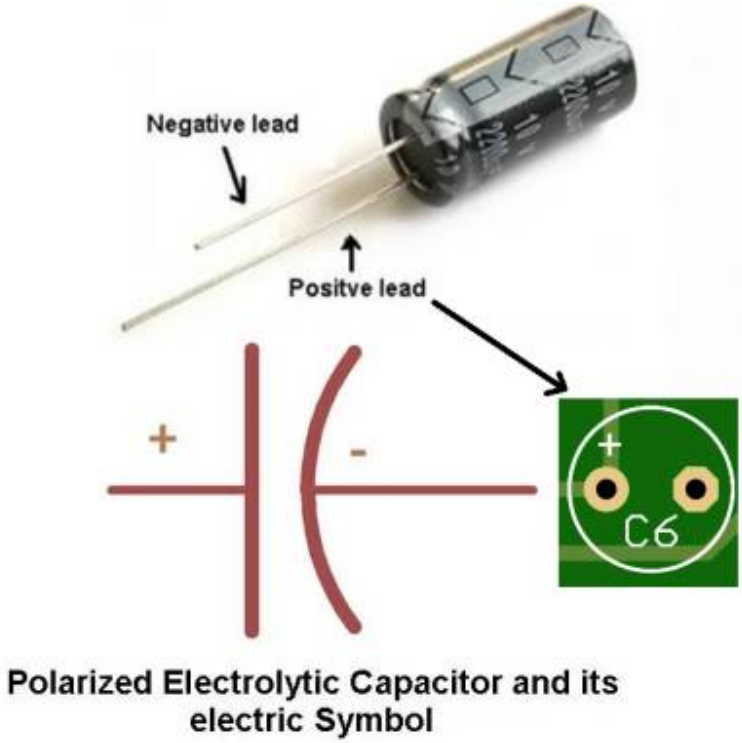
Orientation of “which way is up” doesn’t matter, so you can install them either way. After installation and soldering, do not forget to clip the remaining legs from the PCB.

1.8 Capacitors (electrolytic).

Electrolytic capacitors are small passive components designed to hold a small amount of charge in a circuit.



Electrolytic capacitors are typically polarized, so orientation will matter.

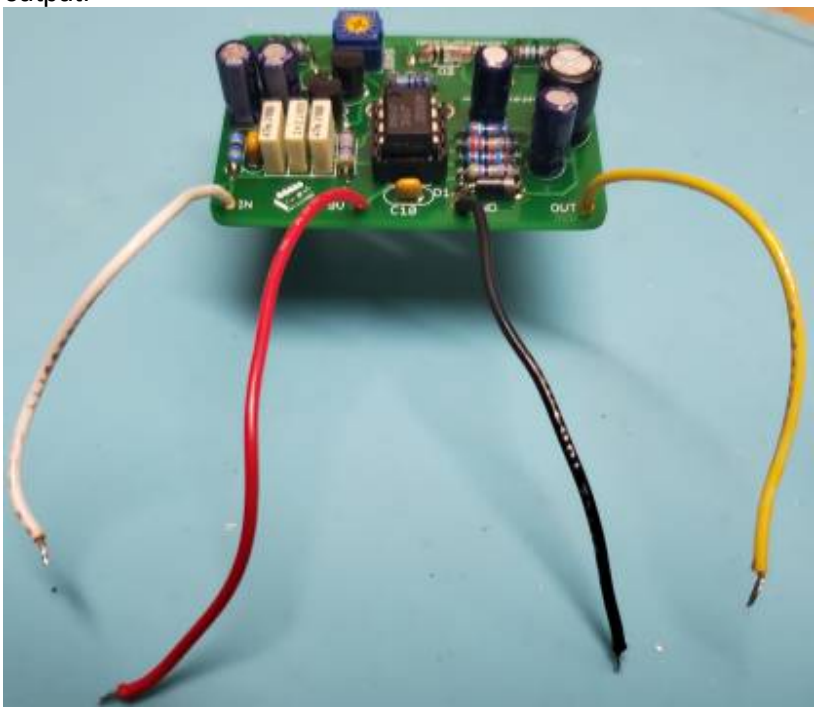


Polarized Electrolytic Capacitor and its electric Symbol

After installation and soldering, do not forget to clip the remaining legs from the PCB.

1.9 Wiring.

Wires used for the pedal are for delivering power over the hot and ground wires as well as signal for the input and output.

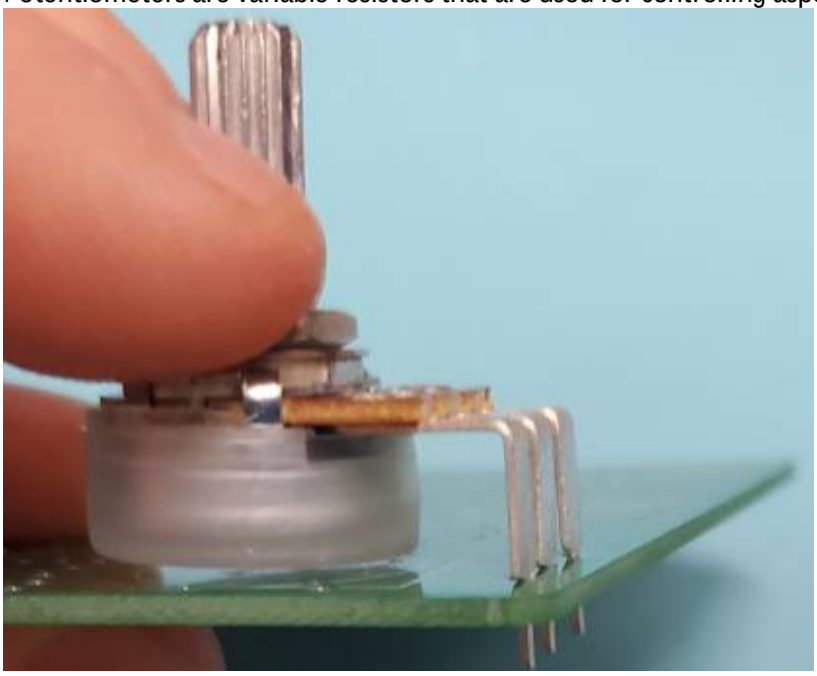


These can be installed at the very end, but in some situations, installing them before potentiometers are soldered in place can be advantageous. Colored wire doesn't change the properties, but using color codes for hot and ground wires, like red being hot, and black being ground, are common place. Typically, stranded hook-up wire, AWG 24 or 22 is used for this task. Using wire strippers, strip away about 1/8" (3mm) of the wire from either end and then using a soldering

iron, tin the exposed tips with solder before installing into the PCB.

1.10 Potentiometers.

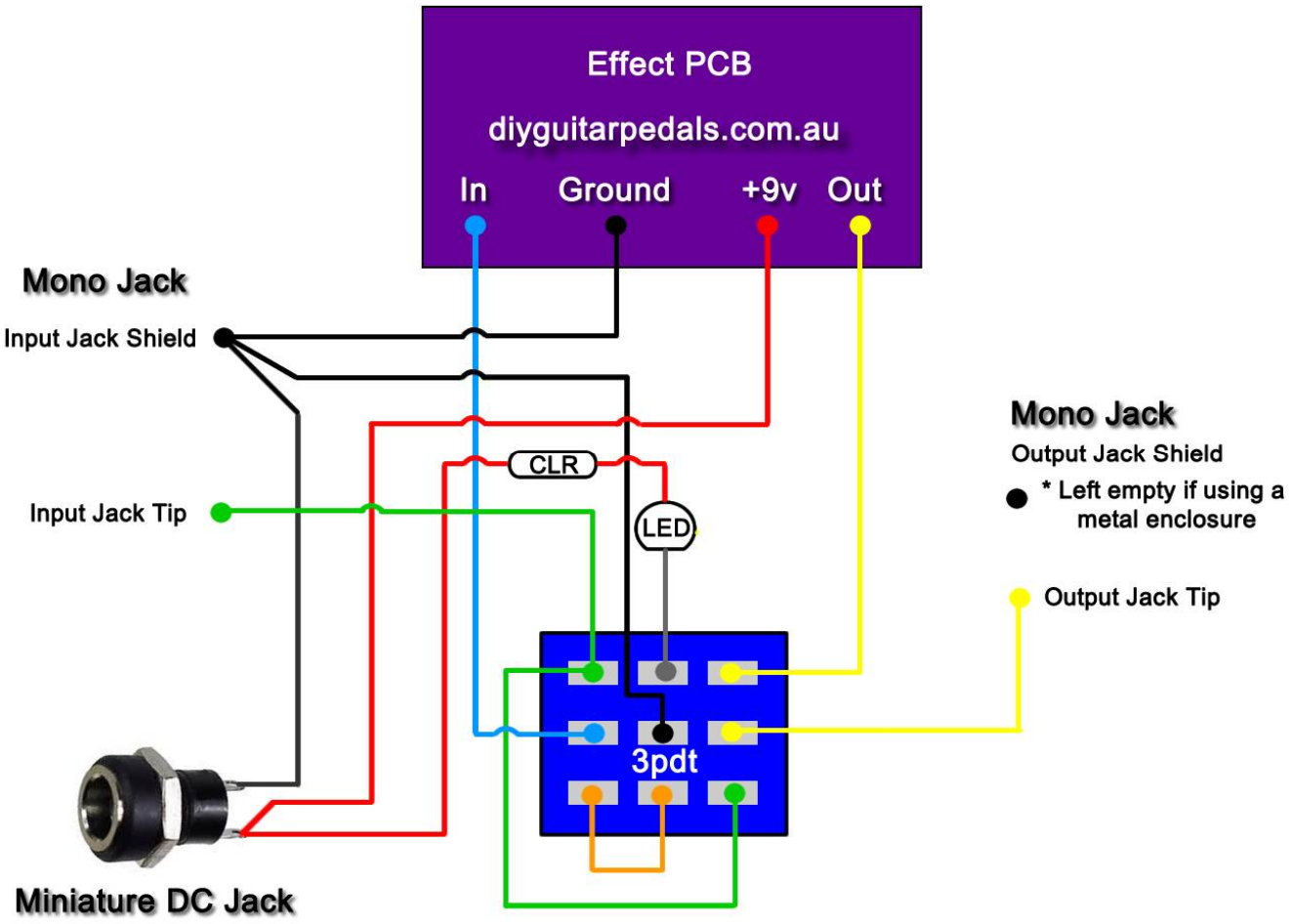
Potentiometers are variable resistors that are used for controlling aspects of the pedal.



This pedal can utilize 16mm pots. These are typically installed on the backside of the PCB and uses the included washer and jam-nut to mechanically secure the PCB to the enclosure via a strategically drilled hole on the enclosure. Orientation of potentiometer is preferred to line up the knob on the silk screen with the knob of the potentiometer.

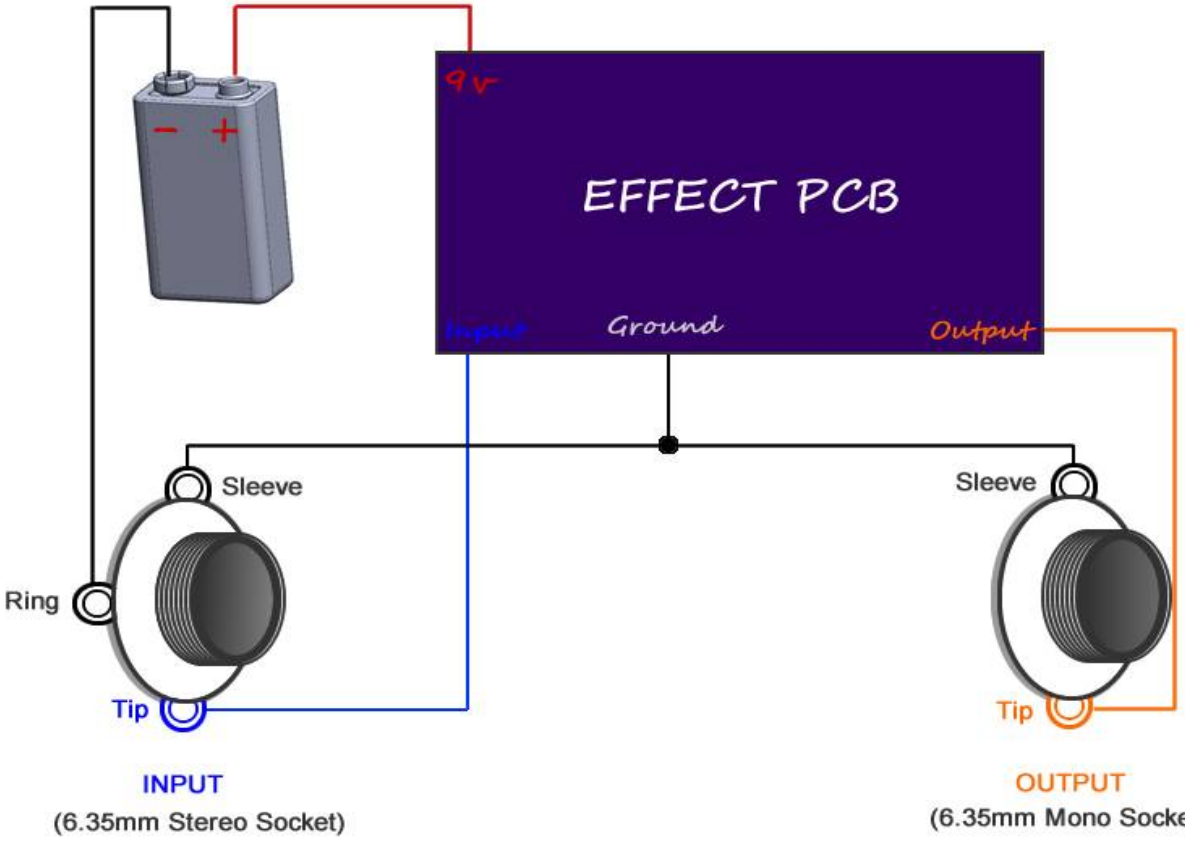
1.11 Off Board Wiring Diagram.

Potentiometers are variable resistors that are used for controlling aspects of the pedal. Using a non-switched miniature DC Jack and 2 Mono Jacks



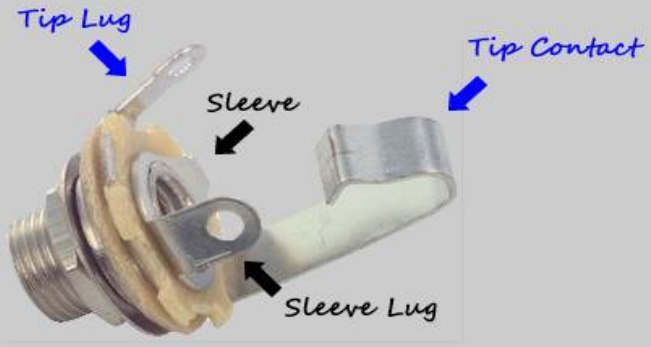
Testing Your Effect

Using aligator clips or soldering directly, wire your effect as in the following...



Input and Output Sockets

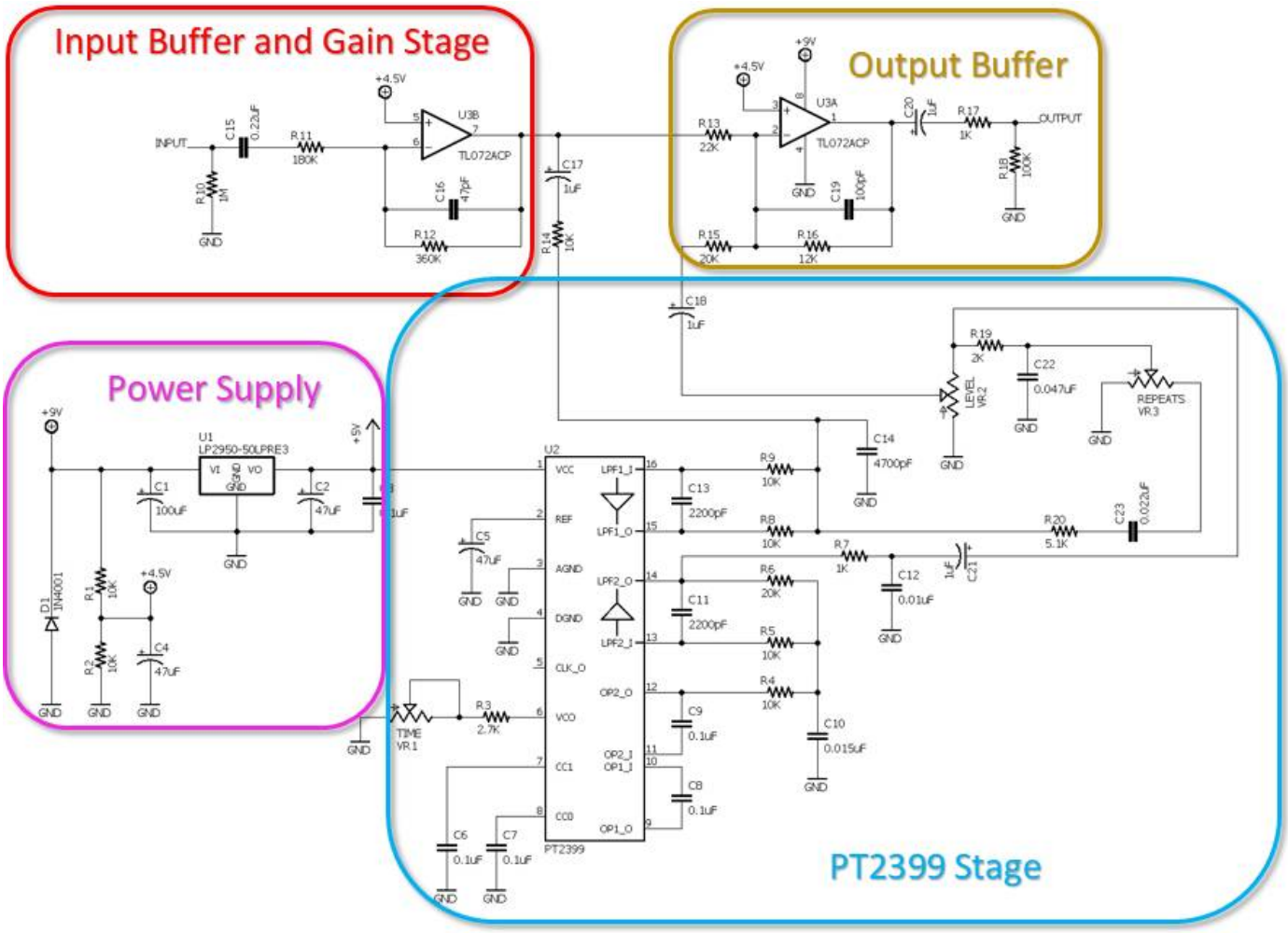
Pay close attention to the lugs of your sockets. Look at them side on so that you can distinguish the sockets individual layers. For instance the tip lug is connected to tip contact. The stereo jack looks the same as the socket below except it has an extra lug and contact for “Ring”.



Boy in Well Circuit Analysis for modifying purposes.

2. Boy in Well Circuit.

The Boy in Well schematic can be broken down into some simpler blocks: Power Supply, Input Buffer and Gain Stage, PT2399 Stage, and Output Buffer.

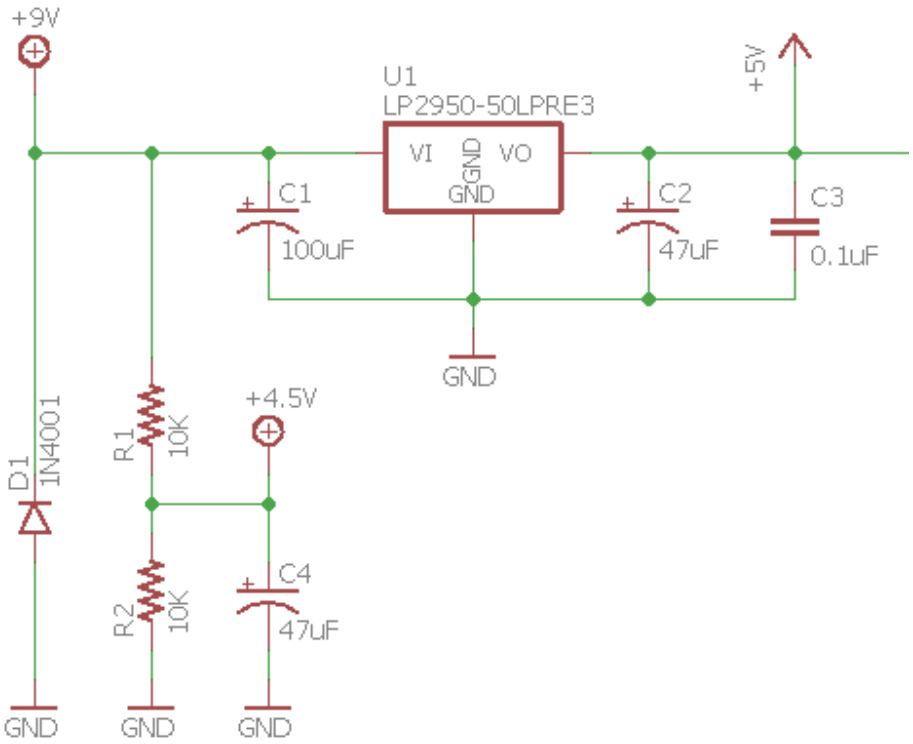


The circuit is designed around a Princeton Technology Corp PT2399 CMOS echo/delay processor with built in ADC, 44Kb of internal RAM, and a DAC.

The input impedance on the Boy in Well is close to 152K Ω, which isn't terrible, but could be improved upon, allowing the pedal to not overload the pickups on the guitar or to tone suck.

3. Power Supply.

The Power Supply Stage provides the electrical power and bias voltage to all the circuitry, the whole power consumption is low and estimated around 8mA:



- The diode D1 protects the pedal against adapter reverse polarity connections.

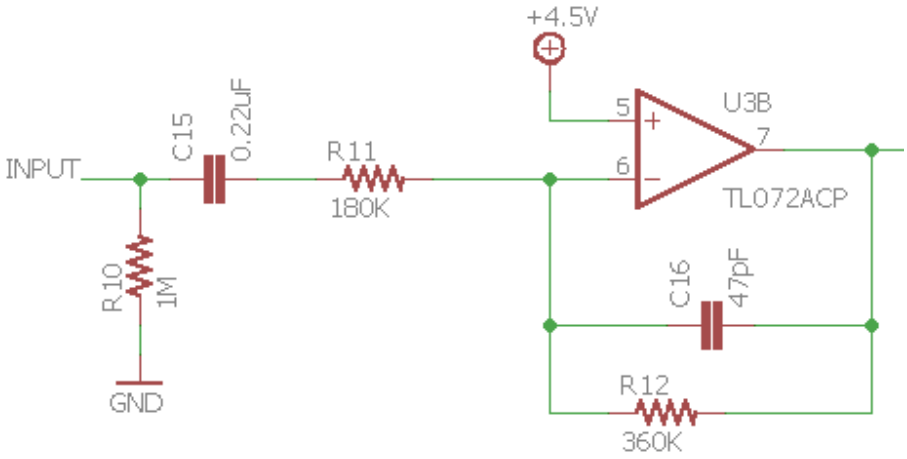
- The resistor voltage divider composed by R1 and R2 generates 4.5V to be used as a bias voltage/virtual ground. The resistors junction (+4.5V) is decoupled to ground with a large value electrolytic capacitor C4 47uF.

- The capacitor C1 is a large electrolytic capacitor to remove ripple from the power supply.

- The LP2950-50LPRE3 is an efficient LM7805 style 5V linear regulator. It is a good idea to get the input capacitor (C1) and output capacitors (C2 & C3) as close to it as possible. It is also a good design rule to get C3 as close to the PT2399, keeping the 5V path short to reject DC line noise. Pairing the C2 electrolytic with the C3 film capacitor helps as electrolytic capacitors are slower in response than film and ceramic capacitors.

4. Input Buffer and Gain Stage.

The first stage is made of an inverting op-amp amplifier with a fixed voltage gain and some filters to shape the gain response and high input impedance that preserves signal quality eliminating tone sucking (high-frequency loss):



The 1MΩ R10 resistor from the input to ground is an anti-pop resistor, it will avoid abrupt pop sounds when the effect is engaged.

The 220nF C15 input capacitor blocks DC and provides simple high pass filtering. C15 and R11 create a high pass filter.

$$fc = 1 / (2\pi RC)$$
$$fc = 1 / (2\pi \cdot R_{11} \cdot C_{15})$$
$$fc = 1 / (2\pi \cdot 180K \cdot 220nF)$$
$$fc = 1 / (2\pi \cdot 180{,}000 \cdot 0.00000022)$$
$$fc = 4.02\ Hz$$

With a cut of 4Hz it will block DC and any low-frequency parasitic oscillation.

4.1 Input Impedance.

The input impedance is defined by the formula:

$$Zin = R_{10} \parallel R_{11}$$

Due to the op amp being configured as an inverting op-amp, the impedance of the op-amp's non-inverting pin is not included.

$$Zin = 1{,}000{,}000 \parallel 180{,}000$$
$$Zin = 152{,}542\Omega$$

Therefore, the Boy in Well input resistance is around 180K, which isn't terrible, but will lead to a darker tone. See the modifications section on how to improve the input impedance, if that is desired.

4.2 Voltage Gain.

The voltage gain is set between the values of R11 and R12, so in a inverting topology this can be calculated as:

$$G_v = R_{12} / R_{11}$$
$$G_v = 360{,}000 / 180{,}000 = 2\ (6dB)$$

4.3 Low Pass Filtering.

The small 47pF capacitor C16 across the feedback resistor works as a low pass filter, softening the corners of the guitar waveform and mellowing out the high end before the clipping.

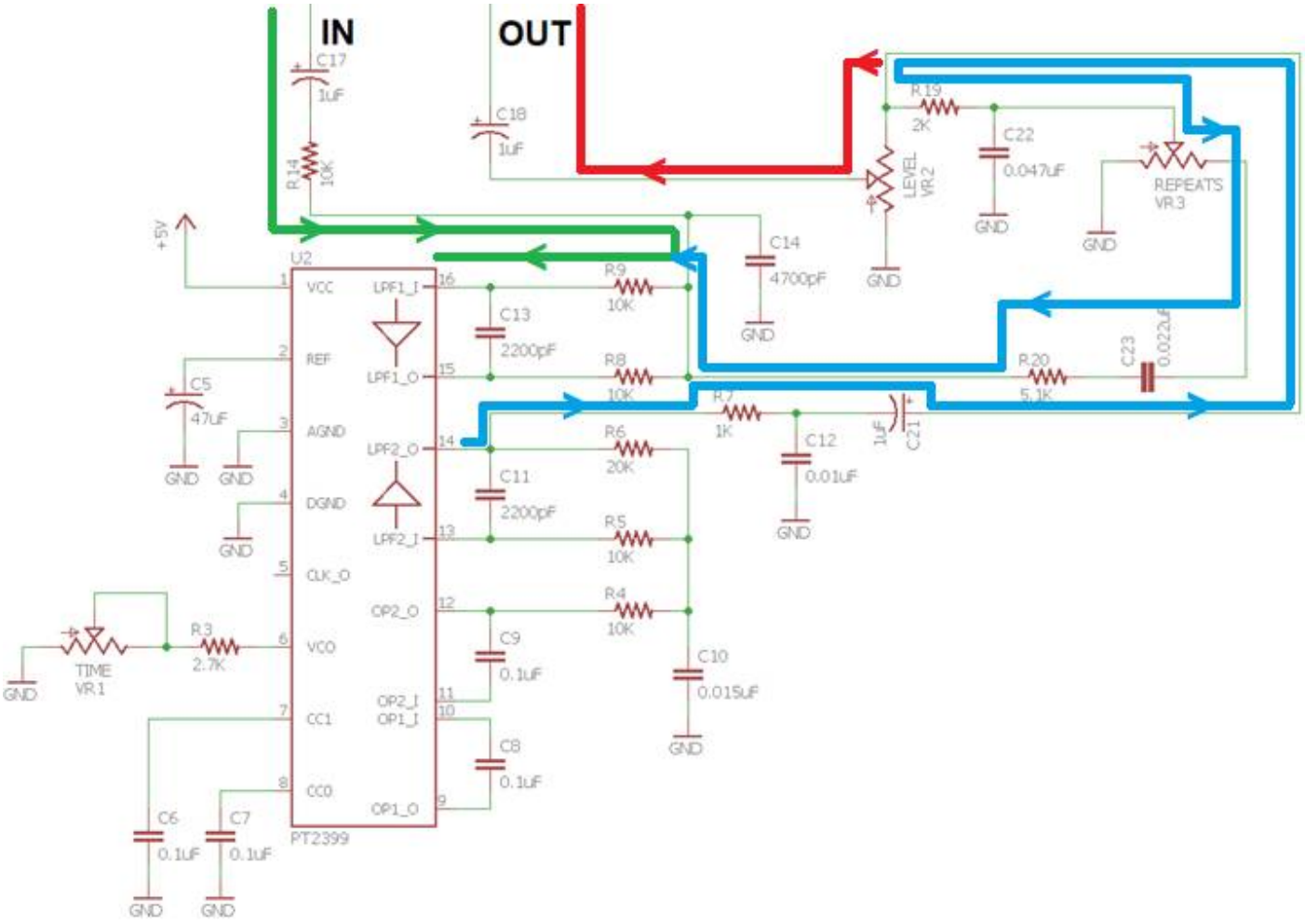
The cut-off frequency of the filter is defined by the formula:

$$fc = 1 / (2\pi \cdot R_{12} \cdot C_{16})$$
$$fc = 1 / (2\pi \cdot 360{,}000 \cdot 0.000000000047) = 9.411\ \text{kHz}$$

This filter cuts off any high frequency harmonics that might occur from a distorted signal that might have been created from the 6dB gain. Not a guarantee that there will be distortion, but if there was, this will filter much of it.

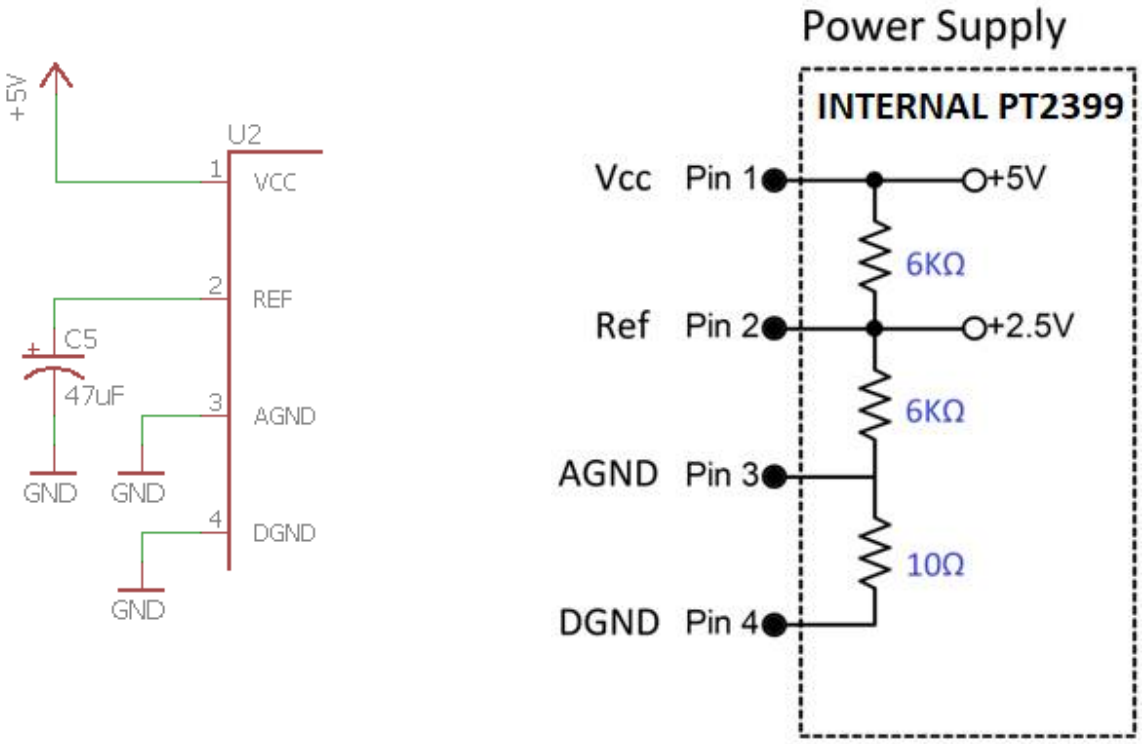
5. The PT2399 Stage.

This stage is taking the prepared buffered audio signal and does all the delaying before outputting the delayed and repeated signal:



5.1 The PT2399 Power Supply

The first 4 pins of the PT2399 are the power supply for the IC:



- **Pin 1** takes in power generated from 5V linear-regulator, U1. The PT2399 can officially handle supply voltages between 4.5V and 5.5V. Some folks have reported success at 6V, but because this would be overclocking and going over the recommended max, it would be important to note if 6V is possible, you don't want to go much higher than that.

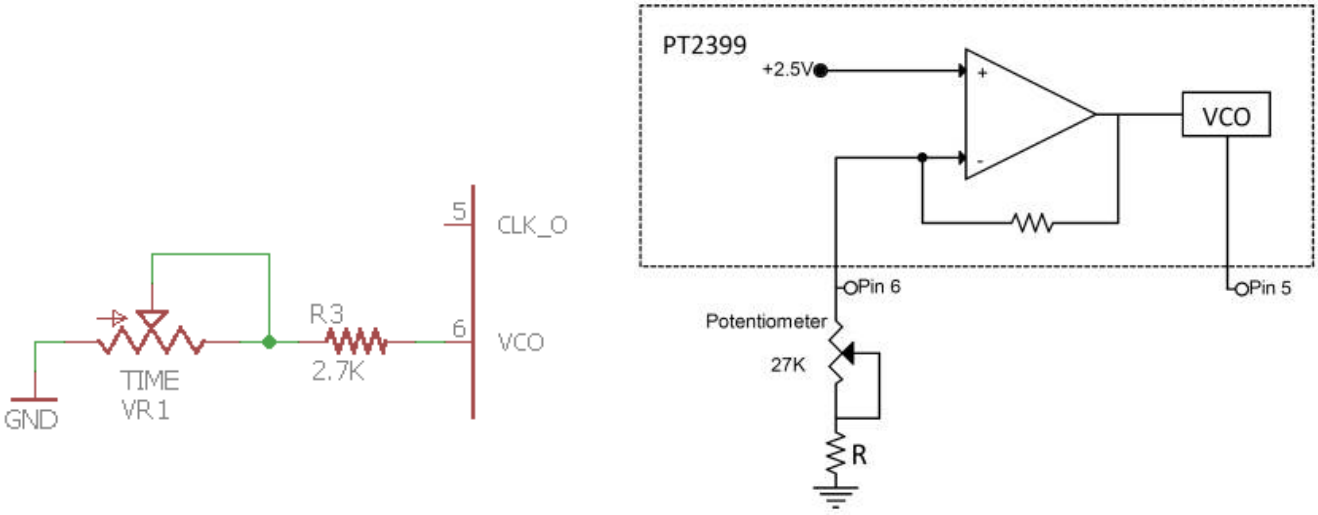
- **Pin 2** is the Ref pin formed by an internal voltage divider of 2x 6K resistors. This creates a voltage reference that is half of the input voltage and is used to create a virtual ground inside the PT2399 and function as a bias reference voltage for its internal VCO circuit. Like a typical pedal circuit, this voltage reference is decoupled to ground with a large value electrolytic capacitor C5 47uF.

- **Pin 3** is the analog ground for the PT2399. This creates ground for the internal VCO, internal Op Amps, and internal comparator inside the PT2399. By using a ground plane on the PCB, we keep a very short, but thick trace between Pin 3 and Pin 4.

- **Pin 4** is the digital ground for the PT2399. It is internally connected to analog ground via an approximate 10 ohms of resistance. This creates ground for the delay propagating circuitry. By using a ground plane on the PCB, we keep a very short, but thick trace between Pin 3 and Pin 4.

5.2 The PT2399 Voltage Controlled Oscillator

Pins 5 and 6 make up the output and input of the VCO or Voltage Controlled Oscillator:



- **Pin 5** is the system clock output pin. The output of this pin is a square wave with a frequency based off the delay time. At its shortest delay, the square wave is at 22 MHz, which is a delay of approximately 30ms. At its longest delay, the square wave is at 2 MHz, which is a delay of approximately 340ms. The signal is approximately 5 Vpp, but it will increase as the frequency decreases and decrease as the frequency increases. This can be used as a feedback for measuring precise delay as simply changing the resistance on Pin 6 will not give an exact delay value. As this is high frequency (22 MHz potentially), a pre-scaler may be desired to read this output from the PT2399 VCO. This would most likely be something good for a microcontroller that could visually display the delay times. This would also be useful to read if trying to synchronize the delay with some other equipment. It is also possible to override the VCO with an external source.

- **Pin 6** is the VCO frequency adjustment pin. The voltage at this pin is always 2.5V and using an external resistor to ground the current will change that will result in a VCO variation and delay time change.

  Find below a table with the relationship between Pin 6 resistance to ground, internal clock frequency, delay time and THD. The table is indicative, as the values vary from chip to chip, however it is a good starting point.

R	27.6 k	21.3 k	17.2 k	14.3 k	12.1 k	10.5 k	9.2 k	8.2 k	7.2 k	6.4 k
f clock	2.0 M	2.5 M	3.0 M	3.5 M	4.0 M	4.5 M	5.0 M	5.5 M	6.0 M	6.5 M
Delay	342 ms	273 ms	228 ms	196 ms	171 ms	151 ms	137 ms	124 ms	114 ms	104 ms
THD	1%	0.80%	0.63%	0.53%	0.46%	0.41%	0.36%	0.33%	0.29%	0.27%
R	5.8 k	5.4 k	4.9 k	4.5 k	4.0 k	3.4 k	2.8 k	2.4 k	2.0 k	1.67 k
f clock	7.0 M	7.5 M	8.0 M	8.5 M	9.0 M	10 M	11 M	12 M	13 M	14 M
Delay	97 ms	92 ms	86 ms	81 ms	76 ms	68 ms	62 ms	57 ms	52 ms	48 ms
THD	0.25%	0.25%	0.23%	0.22%	0.21%	0.19%	0.18%	0.16%	0.15%	0.15%
R	1.47 k	1.28 k	1.08 k	894	723	519	288	0.5		
f clock	15 M	16 M	17 M	18 M	19 M	20 M	21 M	22 M		
Delay	46 ms	43 ms	41 ms	38 ms	37 ms	34 ms	33 ms	31 ms		
THD	0.15%	0.14%	0.14%	0.14%	0.13%	0.13%	0.13%	0.13%		

Note: The THD (Total Harmonic Distortion) is higher with longer delay times, as the signal goes degraded with a lower sampling rate. Using delays over 350ms can cause audible distortion.

Note: The voltage on pin 6 is constant (2.5V) but the current flowing out of it current has a linear relationship with the delay time. The practical delay range of the chip is from about 35 msecs to 600 msecs, so this gives a current of between 5.4mA and 50uA.

Pin 6 current (mA) = 28.65 / (Delay msecs - 29.70)

Note: If delay resistance from Pin 6 to ground is less than 2KΩ during the power-on of the PT2399, the chip may latch up, causing the chip to crash and stop functioning. If a very short delay time is required, ensure that the delay resistance is greater than 2KΩ for the first 400ms after power on. After the first 400ms, the Pin 6 resistance to ground can go as low as needed.

Controlling the Delay Time: Between VR1, a 50K potentiometer and R3, a 2.7K resistor, a minimum resistance of 2.7K is achieved preventing a lock-up of the PT2399 at power on and a maximum delay of 52.7K creating a range of delay between 60ms and 633ms. These can be calculated by:

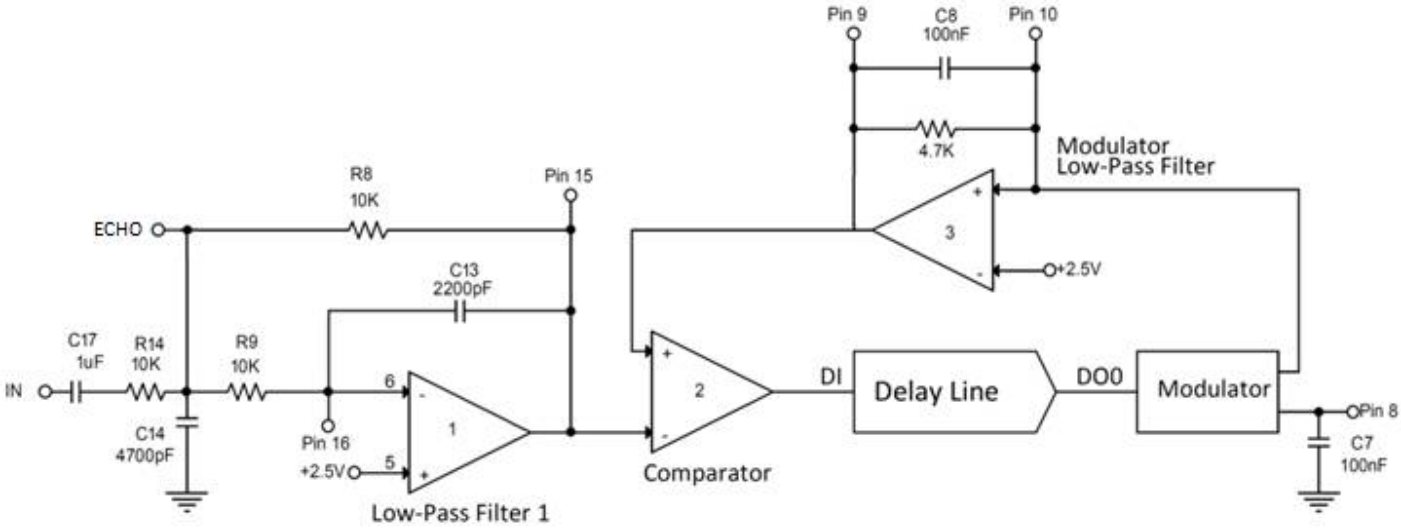
$$Delay_{msecs\ MIN} = (0.01146 \cdot (VR_1 + R_3)) + 29.70$$
$$Delay_{msecs\ MIN} = (0.01146 \cdot 2{,}700) + 29.70$$
$$Delay_{msecs\ MIN} = 30.942 + 29.70 = 60.642\ ms$$

$$Delay_{msecs\ MAX} = (0.01146 \cdot (VR_1 + R_3)) + 29.70$$
$$Delay_{msecs\ MAX} = (0.01146 \cdot 52{,}700) + 29.70$$
$$Delay_{msecs\ MAX} = 603.942 + 29.70 = 633.642\ ms$$

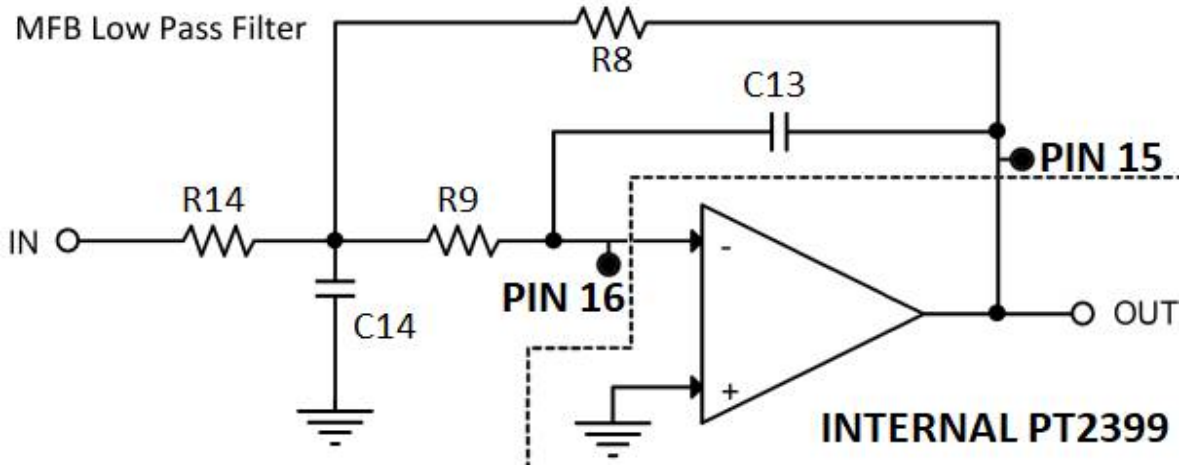
If using an external microcontroller with a digital potentiometer, such as the TAP-FLO and Tap Tempo, so long as the microcontroller takes into consideration power on time and latch potential due to low resistances, after a successful power on, making R3 as small as 100 ohms is possible giving a minimum delay of close to 30 ms.

5.3 PT2399 Input Stage.

The PT2399 Input Stage consists of 3 op-amps. Two of them (2 and 3) are always used as part of the Sigma-Delta ADC circuit, so the designer cannot use them freely. The first op-amp is available to be used under any configuration, but the most common option is to use it as a filter/adder in a Multi-Feedback topology:



The first op-amp will filter the input stage removing the excess of high harmonics using a Multi-Feedback topology (MFB aka *Infinite-Gain Multiple-Feedback*):



The Multi-Feedback op-amp uses 2 poles (MFB-2) that give -12dB/octave of attenuation to the high-frequencies. The final filter (Internal 4.7K resistor and C8) adds an extra pole, making the total filter -18dB/octave. The MFB topology gives high gain / high Q with the inconvenient of more complex design calculations.

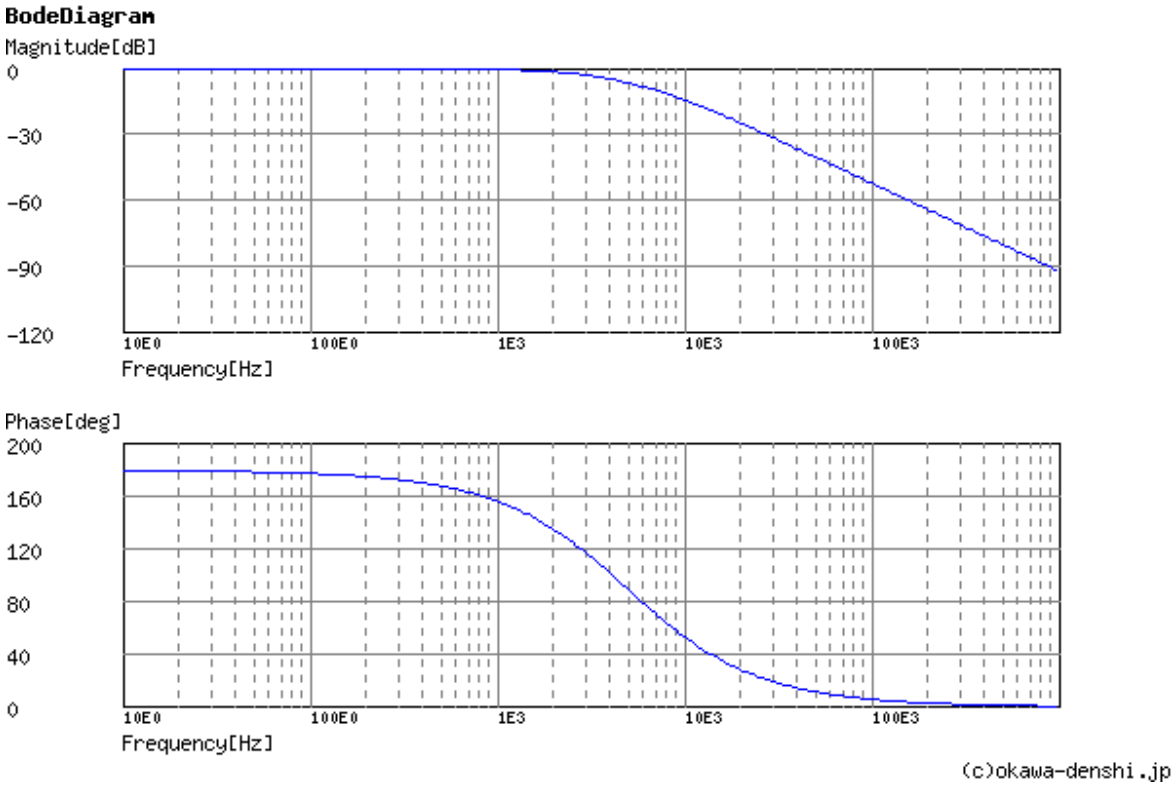
The MFB performs as good as a Sallen & Key filter (S&K uses 1 component less for unity gain filters though) but the MFB topology is chosen in this case it allows the op-amp to work as a summing amplifier, accepting a feedback path of the ECHO circuit.

There are several ways to calculate the values for the filter. Following the simple Elliot Sound Products method, it can be done like this:

R8 = 10K
R9 = 10K
R14 = 10K
C13 = 2.2nF
C14 = 4.7nF

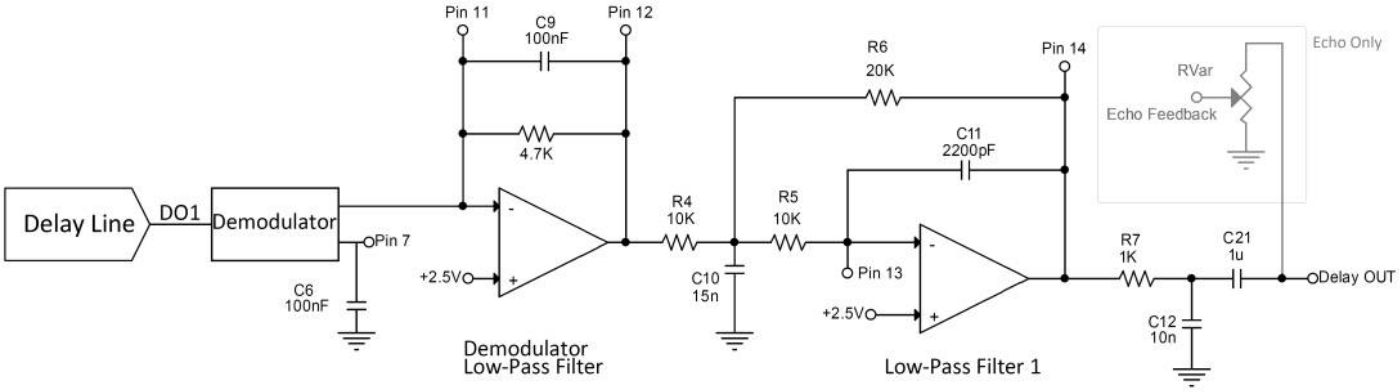
For a simpler calculation, try and keep R8, R9, and R14 the same value, typically 10K. This way a simpler RC filter equation can be used (we can ignore R14 in the equation, so long as R8 = R9 = R14)

$$fc = 1 / (2\pi \cdot \sqrt{(R_8 \cdot R_9 \cdot C_{13} \cdot C_{14})})$$
$$fc = 1 / (2\pi \cdot \sqrt{(10{,}000 \cdot 10{,}000 \cdot 0.0000000022 \cdot 0.0000000047)})$$
$$fc = 1 / (2\pi \cdot \sqrt{0.000000001034})$$
$$fc = 1 / 0.0002020413 = 4949\ Hz$$



5.4 PT2399 Output Stage.

The output stage consists of 2 op-amps. The first one has limited functionality and it is used as a low pass filter after the Demodulator (Anti-Aliasing Filter). The second op-amp is freely available and is again usually configured in a Multi-Feedback op-amp filter.



The output stage uses 1 op-amp as the Demodulator low-pass filter. This Reconstruction Filter will smooth the analog signal created by the Demodulator.

The C9 (and C8) Capacitor forms a low pass filter in order to reduce the unwanted hi-frequencies, the PT2399 datasheet suggests 100nF for delay and 82nF for the echo. There is not much info about the functionality of these caps. Lowering the values of C8 and C9 will allow more high harmonics to go through the chip and therefore a "more natural sound", of course, the drawback would be more digital noise into the signal. If you are using the PT2399 to do short delay/echo you can go as low as 22nF for C8 and C9, for longer delays (300ms) do not go lower than 47nF (100nF seems to be a good value for long delays).

Using 100nF on C8/C9, makes the delayed signal harmonics above 1kHz to be attenuated (see Frequency Response section), it is not catastrophic as the natural sound of a delayed/echoed signal has intrinsically less high content (real echoes usually have a rapidly diminishing high frequency content, as these harmonics are absorbed easily by the walls and air). A good middle ground value to allow more harmonics and less high frequency noise into the circuit would be 68nF.

The second op-amp is again in the Multi Feed Back topology (MFB), it will clean and smooth the signal even more.

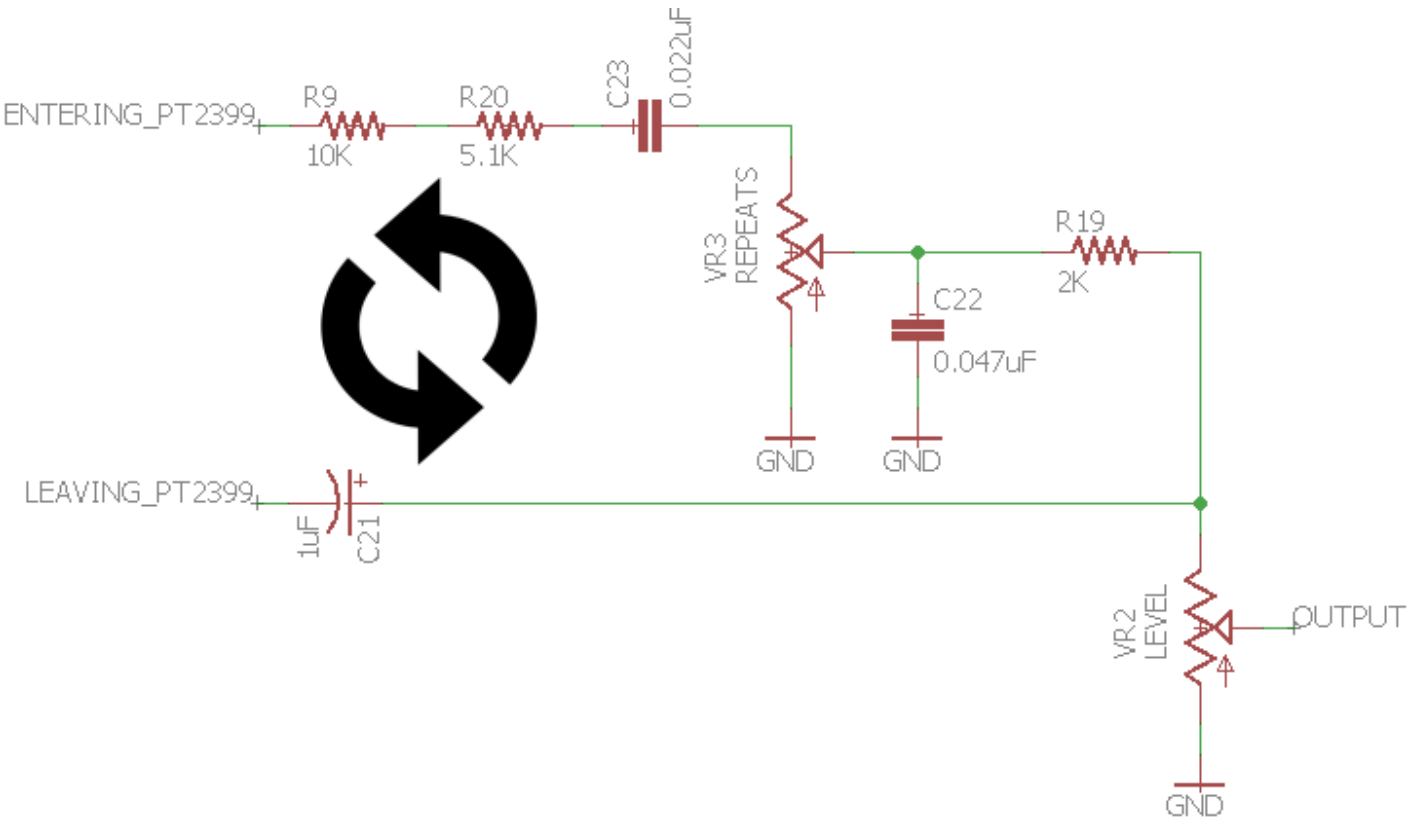
R7 and C12 form a last low pass filter with a cut frequency of 15.9kHz (using a 1KΩ resistor and a 10nF cap) The drawback of this last filter is that it will raise the output impedance of the circuit, this can be solved by using a more sensible RC combination, with a smaller R and a higher C (like 10Ω and 4.7u that give fc=3.3kHz). Thankfully, there is an output buffer that makes this issue mostly irrelevant.

C21 is the output cap that removes any DC level from the output, any big value (1 - 10uF or similar) will work.

5.5 Feedback Loop.

On the first delay output, the PT2399 waits the delay time and sends out a copy of the dry signal. This leaves the Level Potentiometer and then is mixed back with the actual dry signal with the output buffer/summing op-amp U3A. If that were the end of the story, there would only be the original signal with one single delayed signal after it and that would be it. This is what happens as we lower the controls for the VR3 potentiometer, grounding out the repeated signal.

So, to make it echo, we will need to feed the delayed output back into itself.



Assuming the Level knob isn't grounding out the delayed signal, the delay signal is fed back first through a low pass filter, R19 and C22. To calculate the cut-off frequency, the math would look like this:

$$fc = 1 / (2\pi \cdot R_{19} \cdot C_{22})$$

$$fc = 1 / (2\pi \cdot 2{,}000 \cdot 0.000000047) = 1693.1 \text{ Hz}$$

Because this cuts out some of the high frequencies, this makes the repeats "dark". This is also to cover up the distortion limitations of the PT2399. This is reminiscent of how bucket brigade delays work as they have similar distortion limitations.

After it passes through the low-pass filter, it then arrives at the Repeats potentiometer. If not grounded out, the now darker echo passes through a high-pass filter of (R20 + R9) and C23. It can be calculated like this:

$$fc = 1 / (2\pi \cdot (R_{20} + R_9) \cdot C_{22})$$

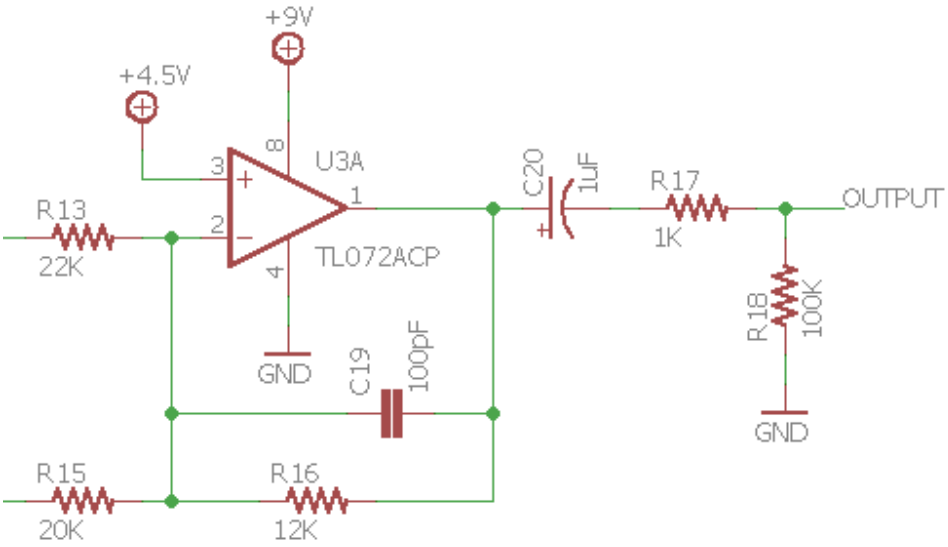
$$fc = 1 / (2\pi \cdot 15{,}100 \cdot 0.000000022) = 479.1 \text{ Hz}$$

This is typically implemented to imitate the poor bass response of the repeats in tape echo. Lowering the capacitor value of C22 removes more of the bass, making it more like a tape echo delay.

6. Output Buffer.

The Output Buffer is the complement of the Input Buffer. It is also implemented over the TL072 dual op-amps and designed to attenuate the magnitude of the high frequencies with respect to the mid-low frequencies. This filter takes the unnatural sounding pre-emphasized audio and turns it back into its original response.

The op-amp is configured in the classic summing amplifier topology. The dry signal coming over R13 has a little more resistance than the dry signal coming in over R15, making the mix ratio 1.1:1 in favor of the wet signal.



6.1 Tone Frequency Response.

A low pass filter is created with R16 and C19.

$$fc = 1 / (2\pi \cdot R_{16} \cdot C_{19})$$
$$fc = 1 / (2\pi \cdot 12{,}000 \cdot 0.0000000001) = 132.7 \text{ kHz}$$

The small 100p C19 capacitor across the feedback loop works as a low pass filter, mellowing out the high end of the signal and limiting the bandwidth which is a classic arrange in stomp boxes input stages that also maintain HF stability.

The Output capacitor C20 acts like a high pass filter together with R17 and R18. Being that R18 is larger than R17, the cut-off frequency is:

$$fc = 1 / (2\pi \cdot R_{18} \cdot C_{20})$$
$$fc = 1 / (2\pi \cdot 100{,}000 \cdot 0.000001) = 1.59 \text{ Hz}$$

This acts to remove DC and any really low frequencies from the output signal.

6.2 Output Impedance.

The input impedance is defined by the formula:
The output resistor network composed by R17 and R18 will limit the output current; even if the output jack is connected to ground the op-amp will see a load of at least 1KΩ, limiting the output current and protecting the operational amplifier. The TL072 op-amp has an internal output resistance of around 100Ω.

The output impedance is defined by the formula:

$$Zin = R_{18} \parallel (R_{17} + Z_{inTL072})$$

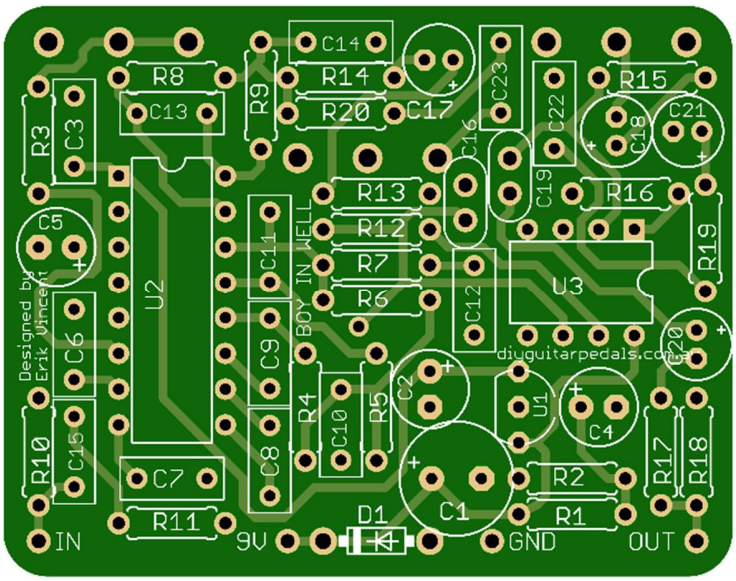
If you look up the datasheet for the TL072, under the electrical characteristics, the input resistance is 10^{12}

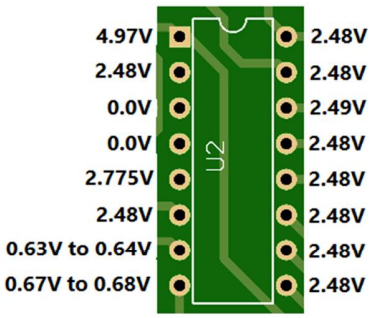
$$Zin = 100{,}000 \parallel (1{,}000 + 100)$$
$$Zin = 100{,}000 \parallel 1{,}100$$
$$Zin = 1{,}088\Omega$$

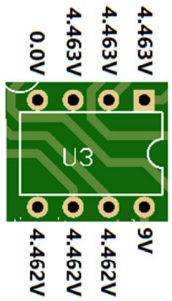
1.088KΩ is good output impedance, keeping signal fidelity. It is a good practice to keep output resistance of a pedal below 10KΩ.

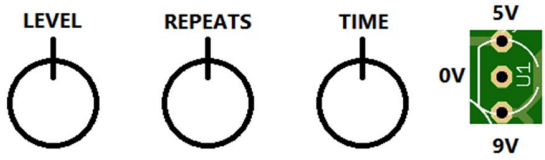
7. Voltage Readings.

Below are the voltage readings of the ICs on the PCB when powered by 9V, engaged, and all knobs set to noon.









8. Modifications

Following is a couple of worthwhile modifications that can be applied to the Boy in Well.

8.1 Resistors

Changing the values of R12 and R11, keeping R12 as the larger value, will increase or decrease the gain created at the input of the signal. At a 2:1 ratio, this creates a voltage gain of 2, or 6dB. Creating a ratio of resistance between R12 and R11 of 3:1 will create a voltage gain of 3, or 9.5dB, 4:1 of 4 or 12dB, and so on. If too much noise is causing mild distortion to the dry signal, creating a ratio of 1:1 creates unity, or 0dB.

The sum of resistance between R3 and the Time pot sets the amount of delay between notes. The lesser the resistance, the shorter in times of delay, getting into reverb/slap-back territory. The greater the resistance, the longer pauses between delays. Remember that a minimum of 2K of resistance is required on the first 400ms of power-up time for the PT2399, so try to keep it above that mark unless a timing method is added off-board. See the chart in section 4.2 for resistance values and delay times.

8.2 Capacitors

C8 and C9 control the harmonics of the delay signal. Lowering the values of C8 and C9 will allow more high harmonics to go through the chip. If you are using the PT2399 to do short delay/echo you can go as low as 22nF for C8 and C9, for longer delays (300ms) do not go lower than 47nF (100nF seems to be a good value for long delays).

C13 and C14 control the MFB low pass filter for processing the delays. Increasing their capacitance will lower the frequency cut off rate, while lowering it will increase the frequency cut-off rate. Values between 330pF – 5600pF can be used.

C23 controls the high-pass filter on the delayed repeats. Lowering the value of C23 will remove more of the bass response, imitating tape delay.

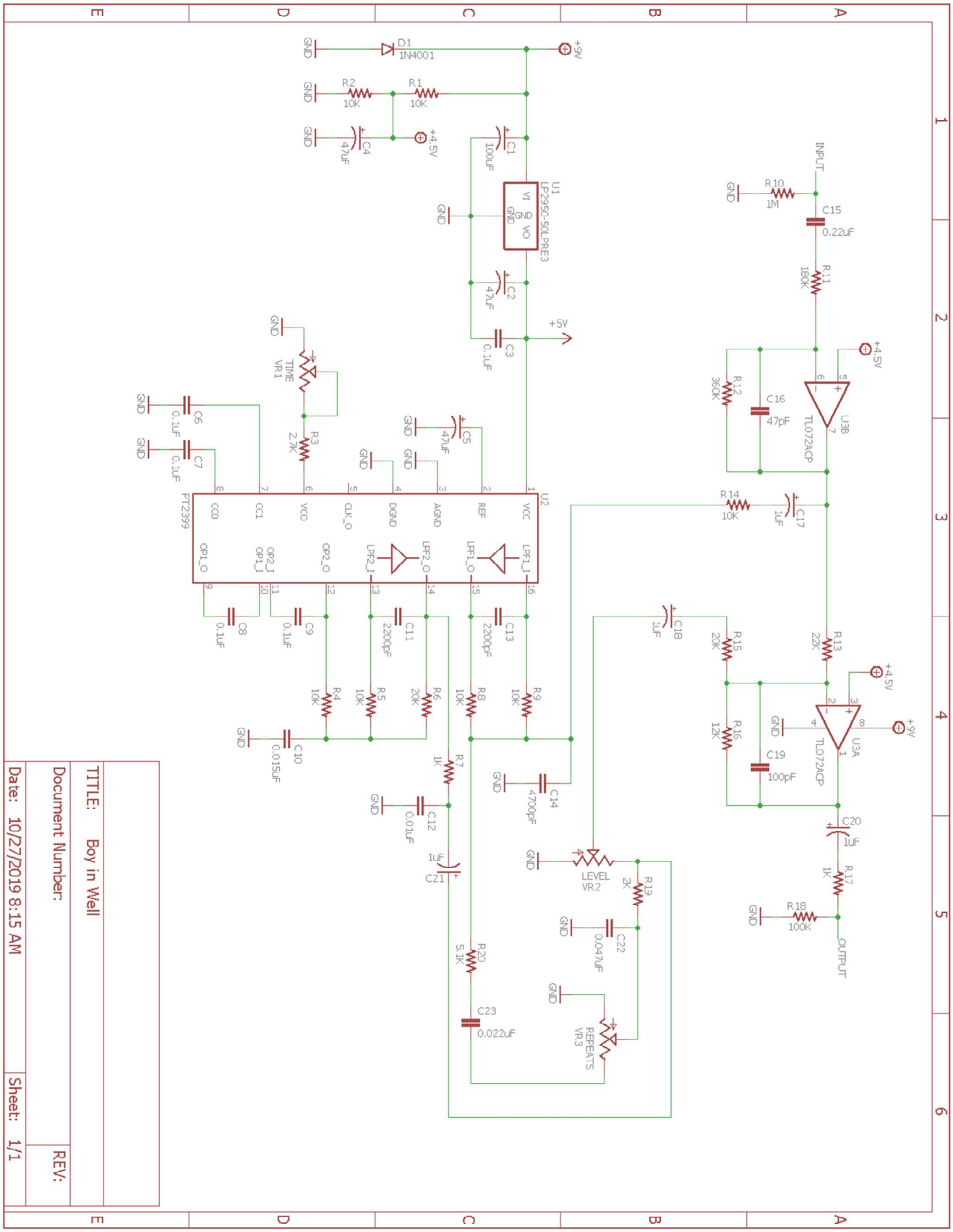
8.3 Voltage Regulators

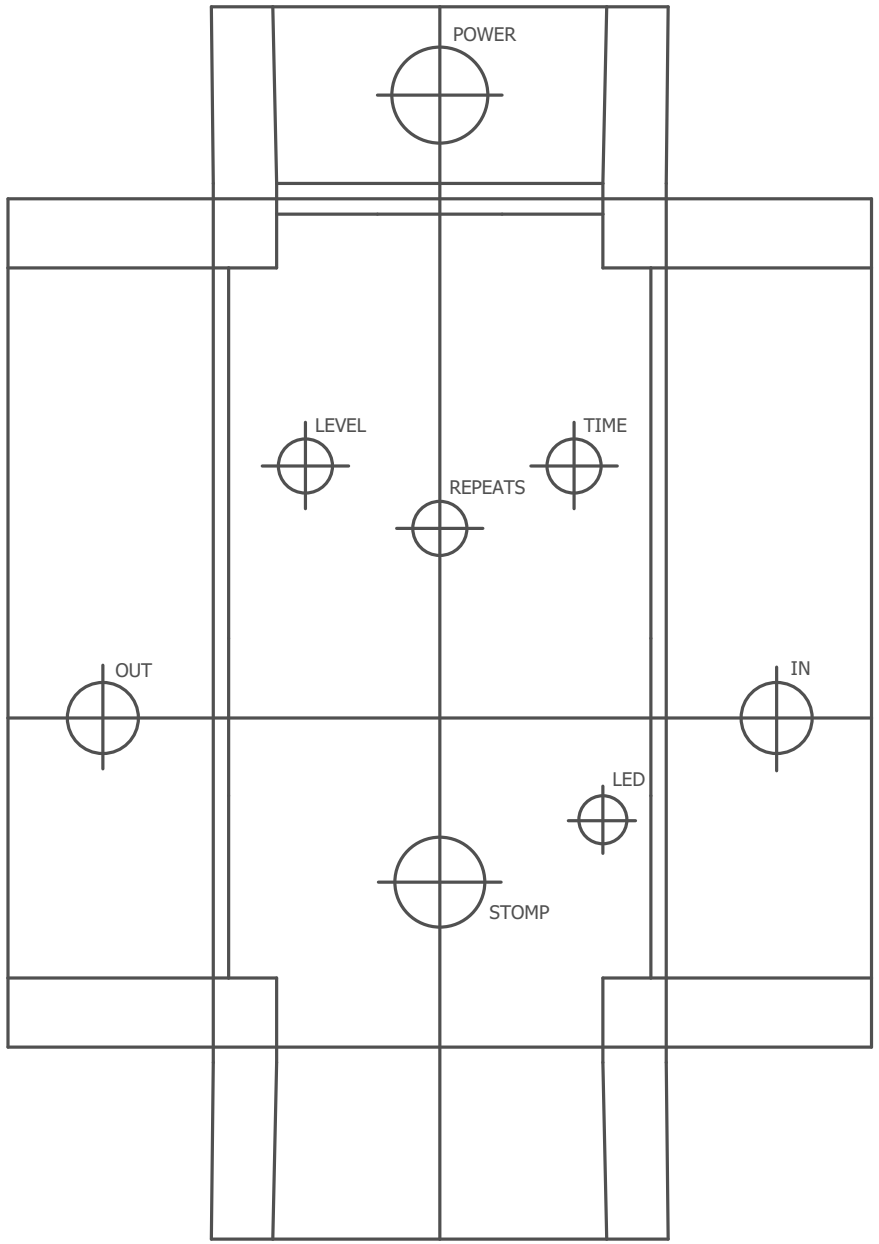
Adapting the Jack Orman's NYE mod, changing the Linear Regulator from a 5V LDO to a 6V LDO such as a 78L06, can make the PT2399 give off a cleaner sounding delay by overclocking the PT2399s internal oscillator. This is just a warning about overclocking. The max voltage for the PT2399 is listed as 5.5V but really pops a little over 6V, so this is pushing the chip to its maximum. Thankfully, due to voltage drops after the regulator, it keeps the circuit relatively safe. Do at your own risk.

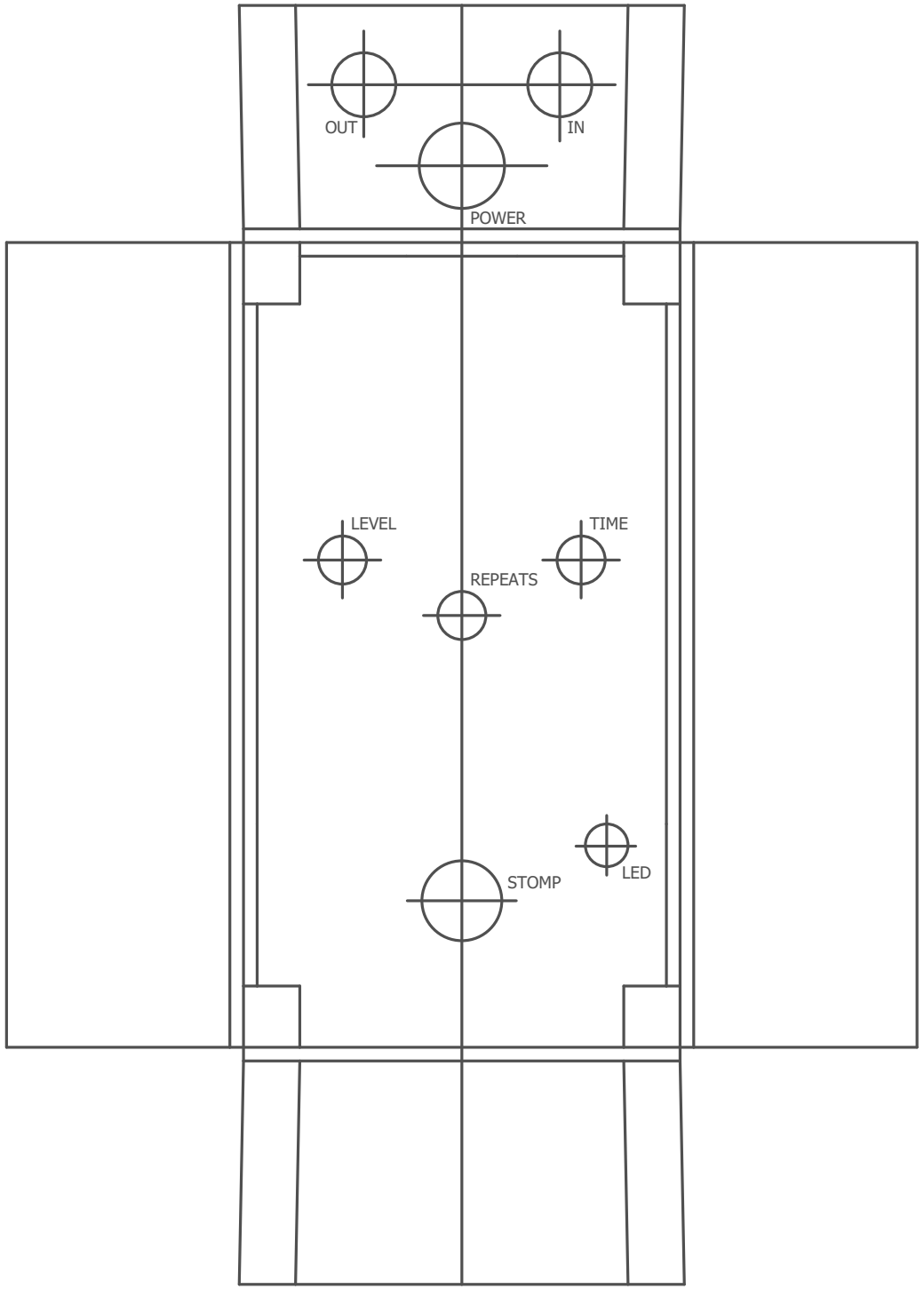
8.4 Input Buffer Bright Mod

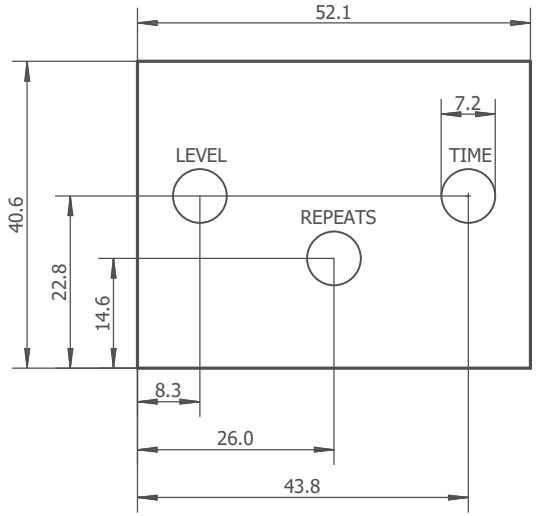
Due to the inverting op-amp of the delay, the input impedance is not as good as it could be. However, to resolve this issue requires a tweaking of a few parts.
R10 needs to become 2.2M
R11 needs to become 1M
R12 needs to become 2.4M
C15 needs to become 33nF
C16 needs to become 6.8pF

9. Schematic


TITLE: Boy in Well
Document Number:
REV:
Date: 10/27/2019 8:15 AM
Sheet: 1/1
D1
1N4001
+9V
R2
10K
R1
10K
C4
47uF
+4.5V
C1
100uF
U1
LP2950-50LPRE3
C2
47uF
+5V
C3
0.1uF
INPUT
R10
1M
C15
0.22uF
R11
180K
R12
360K
C16
47pF
U3B
TL072ACP
TIME
VR1
R3
2.7K
C6
0.1uF
C7
0.1uF
C5
47uF
U2
PT2399
R14
10K
C17
1uF
C18
1uF
R15
20K
R13
22K
R16
12K
C19
100pF
U3A
TL072ACP
C20
1uF
R17
1K
R18
100K
OUTPUT
C8
0.1uF
C9
0.1uF
C11
2200pF
C13
2200pF
R4
10K
R5
10K
R6
20K
R8
10K
R9
10K
C10
0.015uF
R7
1K
C12
0.01uF
C14
4700pF
C21
1uF
LEVEL
VR2
R19
2K
C22
0.047uF
R20
5.1K
C23
0.022uF
REPEATS
VR3


POWER
LEVEL
TIME
REPEATS
OUT
IN
LED
STOMP


OUT
IN
POWER
LEVEL
TIME
REPEATS
STOMP
LED


52.1
7.2
LEVEL
TIME
REPEATS
40.6
22.8
14.6
8.3
26.0
43.8